

Semicustom

CMOS

Standard Cell

CS201 Series

■ DESCRIPTION

The CS201 series of 65 nm standard cells is a line of CMOS ASICs that satisfy demands for lower power consumption and higher integration. These cells offer the minimum level of leakage current in the semiconductor industry, and are able to implement a mixture of core transistors with three different threshold voltages, as appropriate for the applications ranging from handheld terminals to digital audiovisual equipment.

The integration level in this series is twice the previous series with lower power consumption.

■ FEATURES

- Technology : 65 nm Si gate CMOS
6 to 12 layers of metal wiring.
Ultra Low-K (low permittivity) material is used for dielectric inter-layers.
Three different types of core transistors (low leak, standard and high speed) can be used on the same chip.
- Power supply voltage : Supports a wide range from + 0.9 V to + 1.3 V
- Operation junction temperature : - 40 °C to + 125 °C (standard)
- Gate delay time : 11 ps (1.2 V, Inverter, F/O = 1)
- Gate power consumption : 1.77 nW/gate (operating condition: 1.2 V, operating rate 0.5, 1 MHz)
- Reduced chip size achieved by creating the wire bonding pads within the I/O macro regions.
- Support various cell sets (from low power versions to high speed versions)
- Compiled cell (RAM, ROM, others)
- Support large capacity memory "1T-SRAM-Q^{®**1}"
"1T-SRAM-Q[®]" is the embedded memory which enable maximum 128Mbit.
- Support low-consumption technology "CoolAdjust^{™**2}"
- Support ultra high speed (up to 10 Gbps) interface macros
- Special interfaces (LVDS, SSTL, others)
- Short-term development using a physical prototyping tool
- One pass design using a physical synthesis tool
- Hierarchical design environment for supporting large-scale circuits
- Support Signal Integrity, EMI noise reduction
- Support static timing sign-off

(Continued)

CS201 Series

(Continued)

- Improve timing convergence by using Statistical Static Timing Analysis (SSTA)
- Design For Manufacturing (DFM) enables stable product-supply and reduced variation
- Optimum package range : FBGA, PBGA, TEBGA, FC-BGA

*1: To realize this memory, the “1T-SRAM-Q[®]” technology by MoSys Inc. was used

*2: “CoolAdjust[™]” is low power solution presented by Fujitsu Microelectronics.

Note : Some of the features are not available yet.

■ MACRO LIBRARIES (including macros currently being prepared)

1. Logic cells (about 400 types)

Library sets having three different threshold voltages of core transistors.

- Adder
- AND
- AND-OR
- AND-OR Inverter
- Buffer
- Clock Buffer
- Decoder
- Delay Buffer
- ENOR
- EOR
- Inverter
- Latch
- NAND
- NOR
- OR
- OR-AND
- OR-AND Inverter
- SCAN Flip flop
- Non-SCAN Flip Flop
- Multiplexer
- Others

2. IP macros

The following macros will be made available for the CS201 series.

CPU/DSP	ARM [™] * cores(ARM7/ARM9/ARM11),Peripherals IP
Mixed signal macro	ADC, DAC, OPAMP, others
Compiled macro	SRAM (1 Port, 2 Port), ROM, product sum calculators
Large capacity memory	1T-SRAM-Q [®]
PLL	Analog PLL

* : ARM is the trademark of ARM Limited.

3. Special I/O interface macro

Interface macro (PHY)	LVDS, SSTL2, SSTL18, PCI, I ² C, others
Interface macro (controller)	USB2.0 Device/host, Serial ATA, PCI-Express, DDR2, HDMI, others

■ COMPILED CELL

Compiled cells are macro cells that can be automatically generated by specifying the bit/word configuration. The following compiled cells are available for the CS201 series (Note that the bit/word ranges for each macro vary depending on the column type).

1. Clock synchronous single-port RAM (1 address : 1 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
2	16 to 160 K	16 to 1 K	1 to 160
4	32 to 640 K	32 to 8 K	1 to 80
8	64 to 640 K	64 to 16 K	1 to 40

2. Clock synchronous dual port RAM (2 address : 2 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	64 to 72 K	32 to 1K	2 to 72

3. Clock synchronous ROM

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
16	256 to 1M	128 to 8 K	2 to 128
64	1K to 1M	512 to 32 K	2 to 32

4. Clock synchronous register file (2 address : 1 read, 1 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
1	16 to 1152	8	2 to 144
1	32 to 18 K	16 to 128	2 to 144

CS201 Series

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{DD}	- 0.5	+ 1.8	V	*2
		- 0.5	+ 2.5		*3
		- 0.5	+ 3.6		*4
		- 0.5	+ 4.6		*5
Input voltage*1	V _I	- 0.5	V _{DD} + 0.5 (≤ 2.5 V)	V	*3
		- 0.5	V _{DD} + 0.5 (≤ 3.6 V)		*4
		- 0.5	V _{DD} + 0.5 (≤ 4.6 V)		*5
Output voltage*1	V _O	- 0.5	V _{DD} + 0.5 (≤ 2.5 V)	V	*3
		- 0.5	V _{DD} + 0.5 (≤ 3.6 V)		*4
		- 0.5	V _{DD} + 0.5 (≤ 4.6 V)		*5
Storage temperature	T _{STG}	- 55	+ 125	°C	
Operation junction temperature	T _J	- 40	+ 125	°C	
Output current*6	I _O	—	16	mA	
Power supply pin current*7	I _D	—	40	mA	

*1 : V_{SS} = 0 V

*2 : Internal gates

*3 : 1.8 V interface on dual-power supply system

*4 : 2.5 V interface on dual-power supply system

*5 : 3.3 V interface on dual-power supply system

*6 : The output current varies depending on the number of wiring layers in the chip and the wiring configuration of the I/O cells. Contact Fujitsu Microelectronics for details.

*7 : The power supply pin current depends on the type of chip frame. For details, contact Fujitsu Microelectronics.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

• Dual power supply

($V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.0 \text{ V} \pm 0.1 \text{ V}$ / $V_{DDI} = 1.2 \text{ V} \pm 0.1 \text{ V}$)

($V_{SS} = 0 \text{ V}$)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	0.9	1.0	1.1	V
			1.1	1.2	1.3	V
“H” level input voltage	3.3 V CMOS Normal	V_{IH}	2.0	—	$V_{DDE} + 0.3$	V
	3.3 V CMOS Schmitt		2.1	—	$V_{DDE} + 0.3$	V
“L” level input voltage	3.3 V CMOS Normal	V_{IL}	-0.3	—	+0.8	V
	3.3 V CMOS Schmitt		-0.3	—	+0.7	V
Schmitt hysteresis voltage		V_H	0.2	—	1.4	V
Operation junction temperature		T_j	-40	—	+125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Note: For LVCMOS 1.8 V and 2.5 V versions, contact Fujitsu Microelectronics.

CS201 Series

■ ELECTRICAL CHARACTERISTICS

• Dual power supply

($V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.0 \text{ V} \pm 0.1 \text{ V}/V_{DDI} = 1.2 \text{ V} \pm 0.1 \text{ V}$)

($V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.0 \text{ V} \pm 0.1 \text{ V}/V_{DDI} = 1.2 \text{ V} \pm 0.1 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_j = -40 \text{ }^\circ\text{C}$ to $+125 \text{ }^\circ\text{C}$)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
H level output voltage	V_{OH}	3.3 V output $I_{OH} = -100 \mu\text{A}$	$V_{DDE} - 0.2$	—	V_{DDE}	V
L level output voltage	V_{OL}	3.3 V output $I_{OL} = 100 \mu\text{A}$	0	—	0.2	V
Input leakage current	I_L	—	-10	—	+10	μA
Pull-up/Pull-down resistor	R_p	Pull-up $V_{IL} = 0 \text{ V}/$ Pull-down $V_{IH} = V_{DDE}$	15	33	70	$\text{k}\Omega$

Note: For LVCMOS 1.8 V and 2.5 V versions, contact Fujitsu Microelectronics.

■ DESIGN METHODS

Fujitsu's Reference Design Flow provides the following functions that help reduce the development time of large scale, high quality LSIs.

- Statistical Static Timing Analysis (SSTA) improves timing convergence.
- Physical Prototyping enables more accurate estimation of highly reliable designs.
- Layout synthesis with optimized timing is realized by Physical Synthesis Tool.
- High accuracy design environment considers drop in power supply voltage, signal noise, delay penalty and crosstalk.
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considers noise.

■ PACKAGES

The CS201 series can use the same packages that were available for the previous series, allowing a smooth transition from previously developed models.

For details of delivery times, contact Fujitsu Microelectronics.

- FBGA packages
- PBGA packages
- TEBGA packages
- FC-BGA packages

CS201 Series

FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,
Shinjuku-ku, Tokyo 163-0722, Japan
Tel: +81-3-5322-3347 Fax: +81-3-5322-3387
<http://jp.fujitsu.com/fml/en/>

For further information please contact:

North and South America

FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
<http://www.fma.fujitsu.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
<http://www.fmal.fujitsu.com/>

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
<http://emea.fujitsu.com/microelectronics/>

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
<http://cn.fujitsu.com/fmc/>

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
<http://kr.fujitsu.com/fmk/>

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
<http://cn.fujitsu.com/fmc/en/>

Specifications are subject to change without notice. For further information please contact each office.

All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU MICROELECTRONICS device; FUJITSU MICROELECTRONICS does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU MICROELECTRONICS assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU MICROELECTRONICS or any third party or does FUJITSU MICROELECTRONICS warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU MICROELECTRONICS assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU MICROELECTRONICS will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.