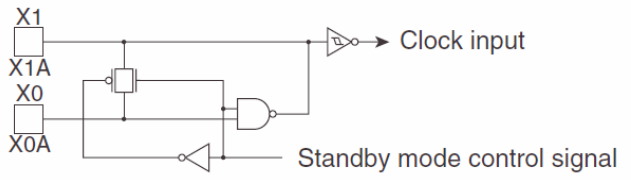
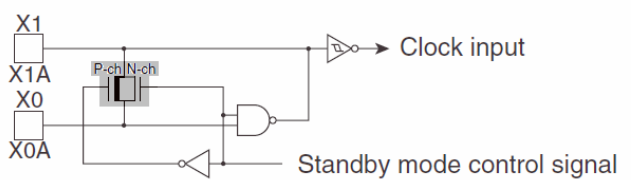
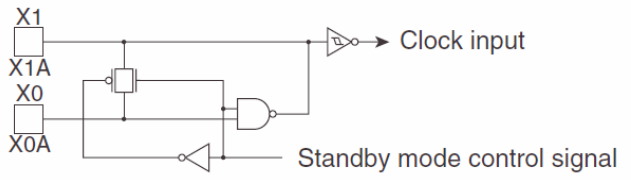
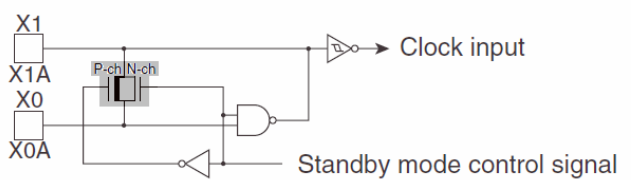
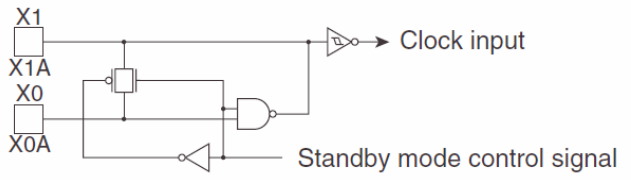
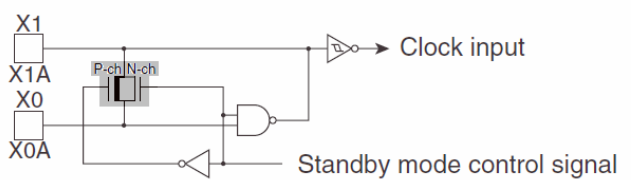


Errata

This errata sheet is for MB90385 Series Hardware Manual Rev.5 (CM44-10118-5E)

F²MC-16LX
 16-BIT MICROCONTROLLER
 MB90385 Series
 HARDWARE MANUAL

2009. 4.2

Date	Page	Item	Description								
2008/8/8	-	-	See the following page for details.								
2009/4/2	14	1.7	<p>The following description of "Classification A" in "Table 1.7-1 I/O Circuit" was corrected as indicated by shading below.</p> <p>(Error)</p> <table border="1" data-bbox="487 745 1372 1008"> <thead> <tr> <th data-bbox="487 745 641 770">Classification</th> <th data-bbox="641 745 1372 770">Circuit</th> </tr> </thead> <tbody> <tr> <td data-bbox="487 770 641 1008">A</td> <td data-bbox="641 770 1372 1008">  </td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1" data-bbox="487 1060 1372 1323"> <thead> <tr> <th data-bbox="487 1060 641 1085">Classification</th> <th data-bbox="641 1060 1372 1085">Circuit</th> </tr> </thead> <tbody> <tr> <td data-bbox="487 1085 641 1323">A</td> <td data-bbox="641 1085 1372 1323">  </td> </tr> </tbody> </table> <p style="text-align: right;">[mcu_doc0872]</p>	Classification	Circuit	A		Classification	Circuit	A	
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Date	Page	Item	Description																																																		
2009/4/2	161	4.3	<p>"Table 4.3-1 Pin Assignment of Port 1" was corrected as indicated by the shading below.</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th rowspan="2">Port Name</th> <th rowspan="2">Pin Name</th> <th rowspan="2">Port Function</th> <th colspan="2" rowspan="2">Resource</th> <th colspan="2">I/O Type</th> <th rowspan="2">Circuit Type</th> </tr> <tr> <th>Input</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td rowspan="4">Port 1</td> <td>P10/IN0</td> <td>P10</td> <td rowspan="4">General purpose I/O port</td> <td rowspan="4">IN0</td> <td rowspan="4">Input capture input</td> <td rowspan="4">CMOS (hysteresis)</td> <td rowspan="4">CMOS</td> <td rowspan="4">D</td> </tr> <tr> <td>P11/IN1</td> <td>P11</td> </tr> <tr> <td>P12/IN2</td> <td>P12</td> </tr> <tr> <td>P13/IN3</td> <td>P13</td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th rowspan="2">Port Name</th> <th rowspan="2">Pin Name</th> <th rowspan="2">Port Function</th> <th colspan="2" rowspan="2">Resource</th> <th colspan="2">I/O Type</th> <th rowspan="2">Circuit Type</th> </tr> <tr> <th>Input</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td rowspan="4">Port 1</td> <td>P10/IN0</td> <td>P10</td> <td rowspan="4">General purpose I/O port</td> <td rowspan="4">TIN0</td> <td rowspan="4">Input capture input</td> <td rowspan="4">CMOS (hysteresis)</td> <td rowspan="4">CMOS</td> <td rowspan="4">D</td> </tr> <tr> <td>P11/IN1</td> <td>P11</td> </tr> <tr> <td>P12/IN2</td> <td>P12</td> </tr> <tr> <td>P13/IN3</td> <td>P13</td> </tr> </tbody> </table> <p style="text-align: right;">[mcu_doc0800]</p>	Port Name	Pin Name	Port Function	Resource		I/O Type		Circuit Type	Input	Output	Port 1	P10/IN0	P10	General purpose I/O port	IN0	Input capture input	CMOS (hysteresis)	CMOS	D	P11/IN1	P11	P12/IN2	P12	P13/IN3	P13	Port Name	Pin Name	Port Function	Resource		I/O Type		Circuit Type	Input	Output	Port 1	P10/IN0	P10	General purpose I/O port	TIN0	Input capture input	CMOS (hysteresis)	CMOS	D	P11/IN1	P11	P12/IN2	P12	P13/IN3	P13
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2009/4/2	166	4.4	<p>■ Configuration of Port 2" was deleted as indicated by the shading below.</p> <ul style="list-style-type: none"> • General-purpose I/O port, resource I/O pin (P20/TIN0 to P27/INT7) • Port 2 data register (PDR2) • Port 2 direction register (DDR2) • High address control register (HACR) <p style="text-align: right;">[mcu_doc0800]</p>																																																		

Date	Page	Item	Description																																				
2009/4/2	226	7.3.1	<p>"Table 7.3-2 Functions of Timer Counter Control Status Register (TCCS)" was corrected as indicated by the shading below.</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th>Bit Name</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>bit 7 IVF: Overflow generation flag bit</td> <td>This bit indicates that the 16-bit free-run timer has overflowed. • If the 16-bit free-run timer overflows or mode setting causes a compare match with the compare register 0 to clear the counter, this bit is set to "1".</td> </tr> <tr> <td>---</td> <td>---</td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th>Bit Name</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>bit 7 IVF: Overflow generation flag bit</td> <td>This bit indicates that the 16-bit free-run timer has overflowed. • If the 16-bit free-run timer overflows, this bit is set to "1".</td> </tr> <tr> <td>---</td> <td>---</td> </tr> </tbody> </table> <p style="text-align: right;">[mcu_doc0800]</p>	Bit Name	Function	bit 7 IVF: Overflow generation flag bit	This bit indicates that the 16-bit free-run timer has overflowed. • If the 16-bit free-run timer overflows or mode setting causes a compare match with the compare register 0 to clear the counter, this bit is set to "1".	---	---	Bit Name	Function	bit 7 IVF: Overflow generation flag bit	This bit indicates that the 16-bit free-run timer has overflowed. • If the 16-bit free-run timer overflows, this bit is set to "1".	---	---																								
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2009/4/2	276	9.3	<p>"Figure 9.3-1 List of Registers and Reset Values of Watch Timer" was corrected as indicated by the shading below.</p> <p>(Error)</p> <table border="1"> <tr> <td>bit</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td></td> <td>1</td> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table> <p>(Correct)</p> <table border="1"> <tr> <td>bit</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td></td> <td>1</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table> <p style="text-align: right;">[mcu_doc0800]</p>	bit	7	6	5	4	3	2	1	0		1	X	0	0	0	0	0	0	bit	7	6	5	4	3	2	1	0		1	X	0	0	1	0	0	0
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Date	Page	Item	Description												
2009/4/2	449	15.3.8	<p>"Table 15.3-10 Functions of Transmission Request Register (TREQR)" was corrected as indicated by the shading below.</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th colspan="2">Bit name</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>bit 7 to bit 0</td> <td>TREQ7 to TREQ0: Transmission request bits 7 to 0</td> <td>--- Read by read modify write (RMW) instruction: "1" is always read. [Setting of remote frame receive wait bit (RFWTR: RFWTx)] ---</td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th colspan="2">Bit name</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>bit 7 to bit 0</td> <td>TREQ7 to TREQ0: Transmission request bits 7 to 0</td> <td>--- Read by read modify write (RMW) instruction: "0" is always read. [Setting of remote frame receive wait bit (RFWTR: RFWTx)] ---</td> </tr> </tbody> </table> <p style="text-align: right;">[mcu_doc0689]</p>	Bit name		Function	bit 7 to bit 0	TREQ7 to TREQ0: Transmission request bits 7 to 0	--- Read by read modify write (RMW) instruction: "1" is always read. [Setting of remote frame receive wait bit (RFWTR: RFWTx)] ---	Bit name		Function	bit 7 to bit 0	TREQ7 to TREQ0: Transmission request bits 7 to 0	--- Read by read modify write (RMW) instruction: "0" is always read. [Setting of remote frame receive wait bit (RFWTR: RFWTx)] ---
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2008/12/9	623	APPENDIX A	<p>■ Table A.9-20 XCH Ri, ea Instruction (First Byte = 7EH) is changed.</p> <ul style="list-style-type: none"> • Error <ul style="list-style-type: none"> Item "A" Line of +A "W2+d16,A" • Correct <ul style="list-style-type: none"> Item "A0" Line of +A "@RW2+d16" 												



Corrections of Hardware Manual

MB90385 - hm90385-cm44-10118-5e-corr-x1-00

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Addendum, MB90385 Hardware Manual (CM44-10118-5E)

This is the Addendum for the Hardware Manual CM44-10118-5E of the MB90385 microcontroller series. It describes all known discrepancies of the MB90385 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90385001	06.12.05	1.00	15	CAN, 'Hit and Away' description added
HWM90385002	06.12.05	1.00		Transition to standby mode, Standby Cancel failure behavior added

Chapter 15. CAN Controller

'Hit and Away' description:

Affected Parts: MB90V495G, MB90F387/S, MB90387/S

Caution for disabling Message Buffers by BVAL bits

1 Caution for Reception

1.1 Behaviour

If there is a complete (no error until 6th bit of EOF) incoming message that have passed the acceptance filter, then this message is stored into a message buffer x (with x=0...15). If this store operation coincides with reset operation of the corresponding BVAL bit (BVALx=0), the received message will be stored into the message buffer 0 regardless of register settings. Note that this coincidence has to happen within a specific CAN-clock cycle (see event 2 in figures). Hence, the probability is very low.

If transmission request of buffer 0 is set (TREQ0=1), the above-mentioned behaviour will lead to the following transmission of a message. This message consists of the received ID, DLC and Data together with original IDE and RTR bits set of the message buffer 0.

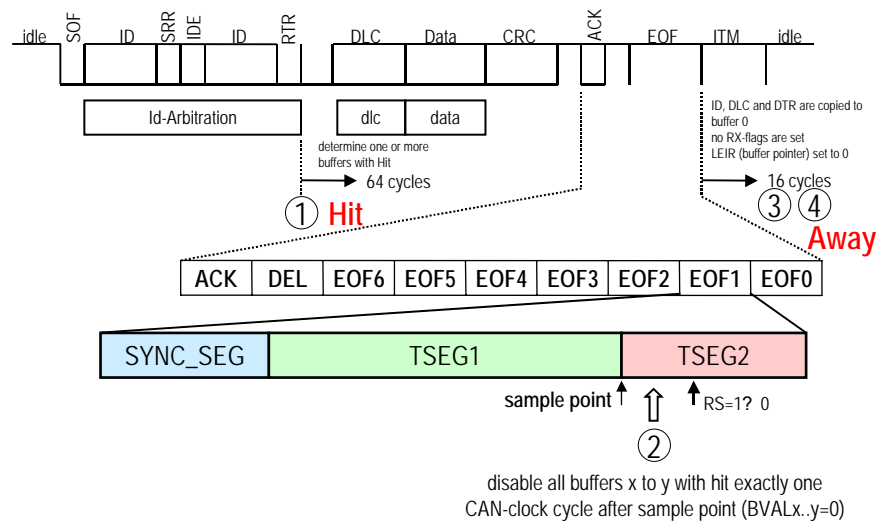
However, if there are two or more message buffers with passing acceptance filer for the incoming message and only buffer x is disabled, the message will be stored into the 2nd prioritised message buffer.

If there are two or more message buffers with passing acceptance filer for the incoming message and all those buffers are disabled, the message will be stored into buffer 0.

1.2 Operation to avoid

When disabling message buffers by the BVAL register, it must be avoided that the write operation to the BVAL register coincides with the store operation of the received message in the CAN Controller.

The following diagram illustrates the timing to be avoided for the BVAL write operation.



- ① CAN-controller determines buffers, which can store the message, because their acceptance filters had been passed.
- ② Software disable all buffers with hit exactly one CAN-clock cycle after the sample point of EOF1.
- ③ CAN-controller stores received ID, DLC and data in buffer 0 regardless of the buffers determined in ①.
- ④ CAN-Controller sets LEIR to point to buffer 0 but RX-flags (RCR, ROVR, RRTRR) are not set.

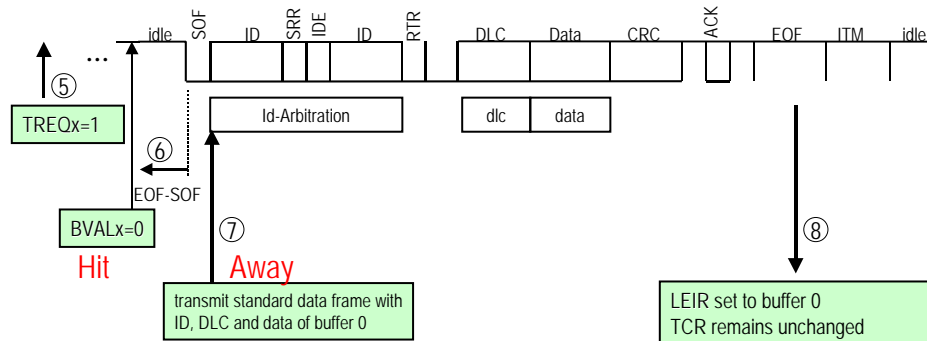
2. Caution for Transmission

2.1 Behaviour

When there is a pending transmission of buffer x and the CAN bus status is in Intermission or in Bus Idle, the CAN-controller will load the message from buffer x in order to send it. If this load operation coincides with disabling the pending message buffer x by clearing the BVAL bit, this results in transmission of a Standard message. This message consists of RTR=0, IDE=0, DLC, 11 ID bits and Data stored in the message buffer 0. Note that this coincidence has to happen with in a specific CAN-clock cycle. Hence, the probability is very low. The position of that cycle depends also on previous frame reception and occurrence of error frames.

2.2 Operation to avoid

When disabling message buffers by the BVAL register, it must be avoided that the write operation to the BVAL register coincides with the preparation for the next transmission in the CAN Controller. The following diagram illustrates the timing to be avoided for the BVAL write operation.



- ⑤ Software requests transmission of buffer x by setting TREQx.
- ⑥ Software disables the buffer x by clearing BVALx.
- ⑦ CAN-controller transmits a standard data frame with ID, length code and data of buffer 0.
- ⑧ After completion of frame only LEIR is updated for buffer 0. However, TCR is not set (neither for buffer 0 nor for buffer x).

3. Correct Operation

3.1 Operation for re-configuring receive message buffers

Depending on CAN applications, it may be necessary to re-configure message buffers after receiving messages through the already active CAN communication. While the CAN bus is active, it is necessary to follow one of the two operations described below to re-configure message buffers by ID, AMS and AMR0/1 register settings. "Active" means that read value of the HALT bit is 0 and the CAN Controller is ready to receive and transmit messages.

1.1.1 Use of HALT bit

Write 1 to the HALT bit and read it back for checking the result is 1. Then change settings for the ID/AMS/AMR0/1 registers.

1.1.2 No use of Message Buffer 0

Do not use the message buffer 0. In other words, disable message buffer (BVAL=0), prohibit receive interrupt (RIE=0) and do not request transmission (TREQ=0).

3.2 Operation for processing received message.

When reading a received message from a message buffer, consideration must be given for possible over-write operation by next incoming messages. Disabling receive operation by the BVAL bit must not be used for this purpose. Use the ROVR bit for checking, if over-writing has been performed. For details, refer to description of ROVR in the hardware manual.

3.3 Cancellation of transmission request

Do not use the BVAL bit for suppressing/cancellation of transmission request. The TCANR bit is prepared for this purpose.

3.4 Composing transmission message

When composing a transmission message by writing to ID, data and other registers, the message buffer should be disabled by the BVAL bit. In this case, the BVAL bit should reset (BVAL=0) after checking if the TREQ bit is 0 or after completion of the previous message transmission (TC=1).

4. Example of avoiding Hit-And-Away

1. Do not use message buffer 0. Keep it always disabled (BVAL0 = 0). By not using buffer 0 the processing of wrongly received messages in buffer 0 is avoided. Even if data are received in this buffer, they have no influence.
2. Set an unused 11-Bit identifier in buffer 0.
"Unused" means that the identifier has no meaning to any node in the network. If an invalid standard data frame is sent according to the condition described in "0
2. Caution for "Transmission", that frame must not cause misoperation of other nodes.
3. Use overrun test while processing a received message.
After temporarily saving received message, test for overrun (ROVRR). If overrun occurred, read the buffer again, because the read data before overrun could be inconsistent.
4. Wait for completion of transmission.
A buffer must not be disabled by clearing the BVAL-flag, as long as there is a pending transmission. Easiest way to wait for transmission completion is to use transmission interrupt but polling of TREQ is also possible.

Transition to standby mode

The definition of Standby Cancel Failure is that the CPU will execute wrong instructions when an interrupt is executed during transition to Standby mode¹ at a certain time

¹:Definition of Standby mode

Main sleep mode, PLL sleep mode, Sub-sleep mode
Time base timer mode, Watch mode, Main watch mode
Main stop mode, PLL stop mode, Sub-stop mode

In the following cases, no problem occurs:

- Standby mode is not used
- Standby mode is released only by external reset

For further information refer to Hardware Manual 'Usage Notes on Low-Power Consumption Mode'.