

# Solutions for FUJITSU NAND Flash Memories

*FUJITSU introduces NAND flash memories, which are ideal for storing large volumes of data. FUJITSU also introduces software, macro, and other solutions that are necessary to incorporate into the systems.*

## Features

- **System tools to support NAND flash use:**
  - **Error checking and correction macro**
  - **Sophisticated flash file system support**
  - **SoLib FAT access library support**
  - **Simulation models**

## Product Overview

FUJITSU already produces a line of NOR flash memory products that meets the need for program code

**“... are easier to design in large-capacity sizes and better suited to data storage ...”**

storage. However, the rapid progress in portable devices has led to intensifying demand for compact, high-capacity memory media for

data storage. FUJITSU has responded to this demand by developing and releasing NAND flash memories. NAND flash memories are easier to design in large-capacity sizes and better suited to data storage than the NOR flash memory.

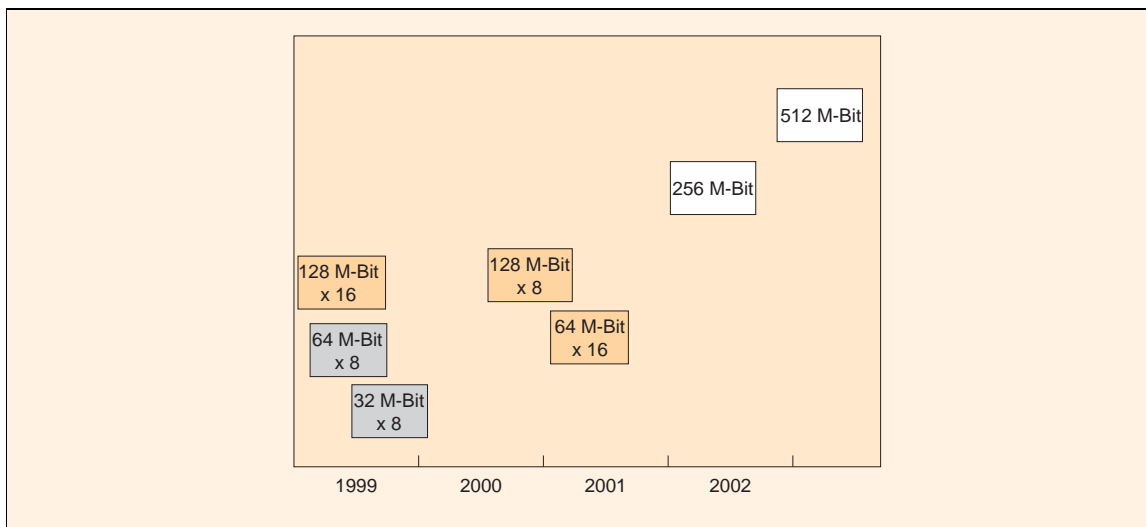
Figure 1 (see p. 4) shows a road map of NAND flash memory development.

Table 1 (see p. 4) shows a comparison of read/write/erase times for NAND flash memories and NOR flash memories. As the data show, the NAND flash memory has faster write/erase times than the NOR flash memory and is better suited for storage of large volumes of data.

Figure 2 (see p. 4) illustrates the use of different flash memories for general applications.

In addition to the flash memory itself, FUJITSU is emphasizing the solutions, including software, information, and tools that allow flash memories to be efficiently and rapidly built into customer products. This article introduces a variety of FUJITSU solutions available for use with NAND flash memories.

**Figure 1. Roadmap of the NAND Flash Memory**

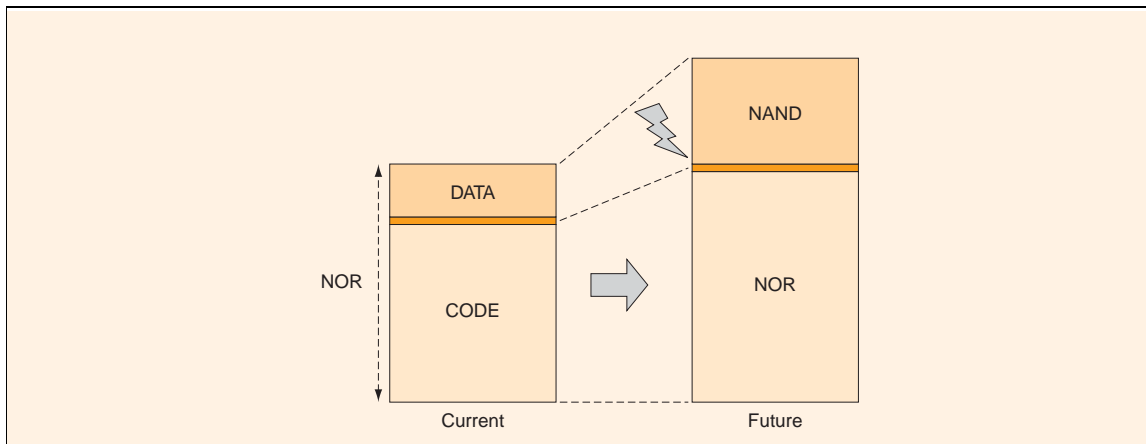


**Table 1. Comparison of NAND Flash Memories and NOR Flash Memories**

|                    | NAND Flash Memory*                                  | NOR Flash Memory                                      |
|--------------------|---|---|
| Read Unit          | Page (512 + 16 bytes)                               | Byte/Word   |
| Access Time (typ.) | 7 $\mu$ s (initial access)<br>50 ns (serial access) | 90 ns (random access)                                 |
| Write Unit         | Page (512 + 16 bytes)                               | Byte/Word   |
| Write Time (typ.)  | 200 $\mu$ s   | 8 $\mu$ s/Byte<br>16 $\mu$ s/Word<br>(4 ms/528 bytes) |
| Erase Unit         | Block (8K + 256 bytes)                              | Sector (8K/64K bytes)                                 |
| Erase Time (typ.)  | 2 ms  | 1s  |

\*In the MBM30LV0064

**Figure 2. Sample Flash Memory by Objective**



# Facts and Features of NAND Flash Memories

The following features and facts should be considered when using NAND flash memories.

## Bad Block Potential

NAND flash memories are subject to a condition called “bad block,” in which a block cannot be completely erased or partial or 1-bit errors prevent write access. Bad blocks may exist in NAND flash memory when shipped or may occur during operation. Supervisory software must detect the occurrence of these bad blocks and manage operation so that a bad block is no longer used. The number of such bad blocks in a 64 M-bit MBM30LV0064 memory is warranted to be no more than ten.

## Bit Error Occurrence During Data Read Operations

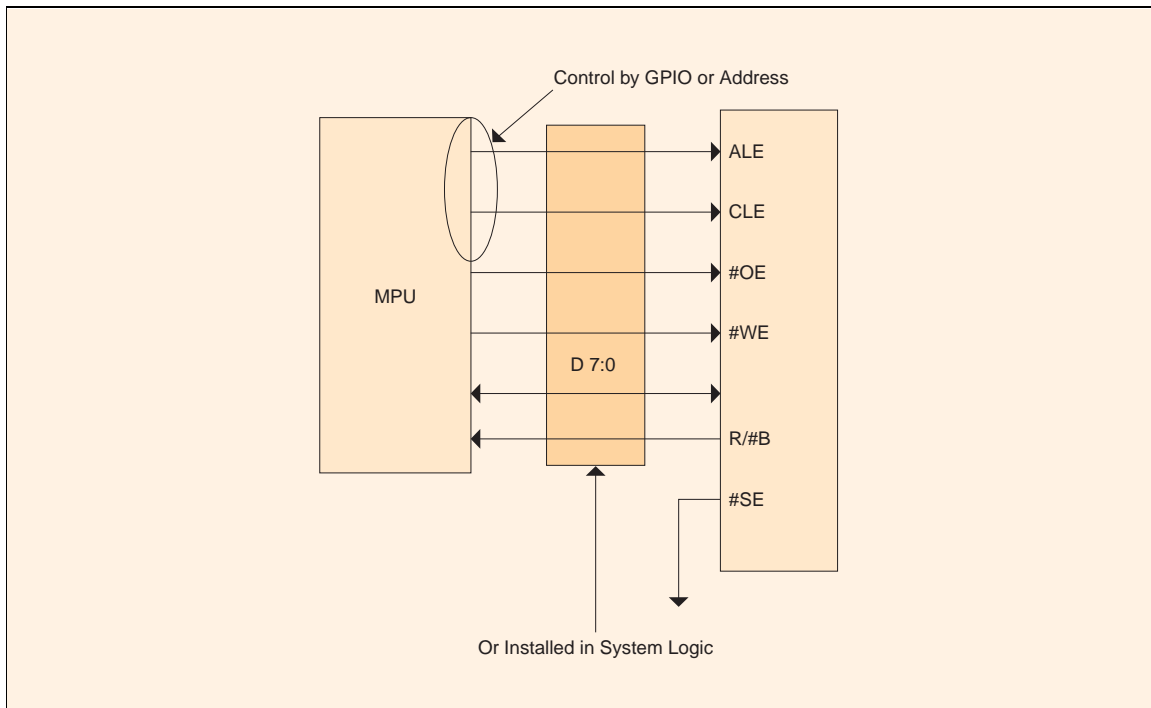
The structure of the NAND flash memory is such that, during read operations as well as write/erase operations, high voltages are applied to the cells that form the units of data storage. This means that during extended periods of use, bit errors can occur while reading. For this reason, we strongly recommend that Error Checking and Correction (ECC) be incorporated into the supervisory software to handle such situations.

## CLE/ALE/SE Pin Control

There are several pins on a NAND flash memory that do not exist on a NOR flash memory, including Command Latch Enable (CLE), Address Latch Enable (ALE), and Spare Area Enable (SE) pins. These pins must be controlled by the host system.

Figure 3 illustrates the connections and control of a NAND flash memory.

**Figure 3. Sample NAND Flash Memory Connection and Control**



**Initial Access Time (relative to a NOR flash memory)**

In serial access operation, NAND flash memories are capable of high-speed access times of 50 ns for read access. The initial access to a page, which is the basic read unit, requires 7 μs. This presents no problems for serial access to files or other data that are grouped in one location, but is not well suited to storage of program code.

Table 2 (see p. 7) summarizes points about NAND flash memories.

## FUJITSU Solutions

The facts we have described above have traditionally been addressed with comments such as “use a commercially available controller,” or “... solutions for our customers, including the following software, macro, and reference resources.”

“using the customer’s system configuration.” Now, however, FUJITSU has developed a set of solutions for our customers, including the following software, macro, and reference resources.

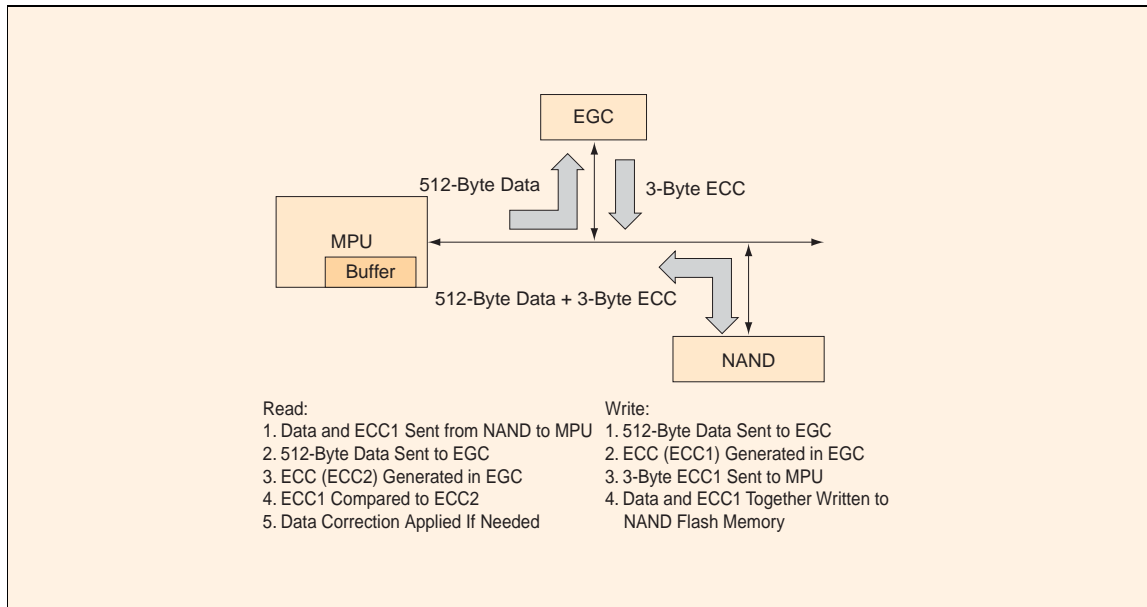
**ECC Macro**

An ECC macro capable of correcting 1-bit errors and detecting 2-bit errors is available in Verilog, VHDL, and C. This is a type of humming code and offers the feature that generates only 3 bytes of ECC code per unit page (512 bytes). This macro can be used either as a hardware macro built into an ASIC in the customer’s product or installed in system logic.

Figure 4 shows examples of ECC macro uses. Specifically, the following are available:

- ECC macro source (Verilog, VHDL, C)
- ECC macro specifications
- ECC macro application note

**Figure 4. Examples of ECC Macro Installation**





**NAND Flash Memory Control Software**

FUJITSU already provides the Sophisticated Flash File System (SoFFS) for NOR flash memory control and now has developed a version of SoFFS for use with NAND flash memories. Designed to stand between the application software and the NAND device, SoFFS offers the following primary functions:

- Wear leveling
- Garbage collection
- Bad block management

In addition, FUJITSU provides the SoFFS FAT Access Library (SoLib), an access library providing a FAT-compatible file system.

Figure 5 (see p. 8) shows an example of SoFFS and SoLib installation. Specifically, the following are available:

- SoFFS for NAND source code
- SoFFS for NAND integrator's manual
- SoFFS for NAND descriptive manual
- SoLib for NAND object code
- SoLib for NAND specifications

**NAND Flash Memory Control and Connection Reference**

As a reference for the control and connection of the CLE, ALE, and SE pins, we offer sample connection

and circuit diagrams for the FUJITSU 32-bit RISC microcontroller FR30. In the examples, those particular pins are controlled by registers. Specifically, the following are available:

- Sample FR30 and NAND flash memory connection specifications
- FR30 and NAND flash memory connection circuit diagrams
- NAND flash memory expansion board for use with an FR30 evaluation board (loan only)

**NAND Flash Memory Simulation Models**

Currently, VHDL, Verilog, IBIS, and Denali models are available for the 64 M-bit MBM30LV0064 flash memory.

Table 3 (see p. 8) lists points to remember when using NAND flash memories, together with solutions provided by FUJITSU.

**Future Development**

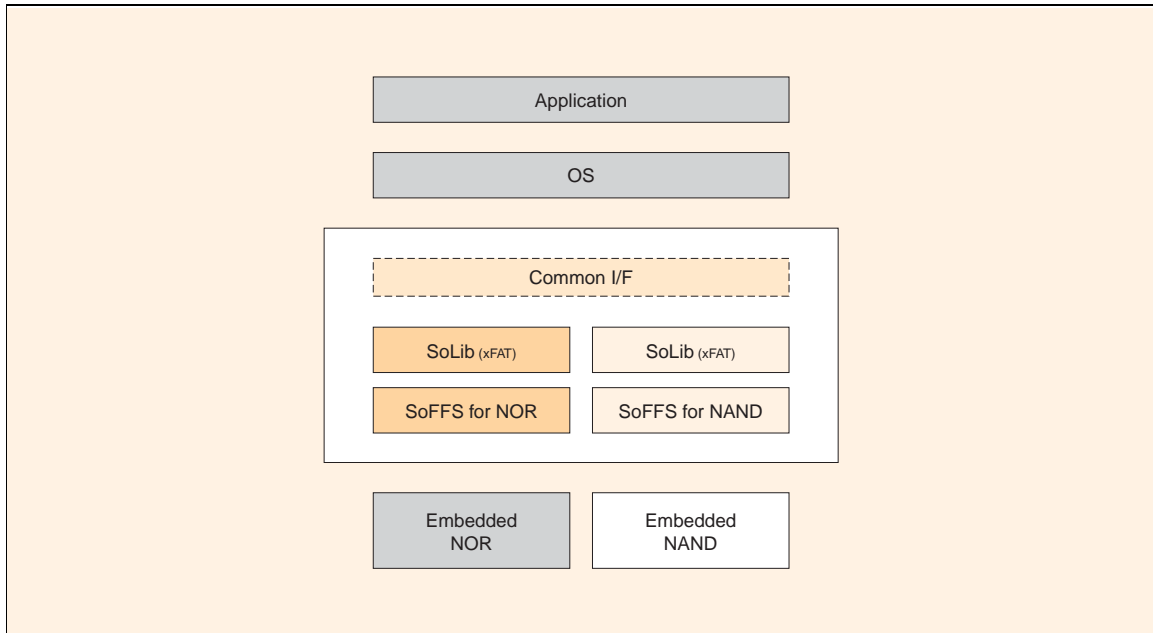
FUJITSU will continue to apply the solutions we have developed to all our NAND flash memories. We will provide customers with not only the memory devices themselves, but also a wide range of solutions and services related to flash memories, including software, tools, models, and other resource information. ◆

**Table 2. NAND Flash Memories System Requirements**

|                             |                      |
|-----------------------------|----------------------|
| Required System Features    | Bad Block Management |
|                             | Specific Pin Control |
| Recommended System Features | ECC Installation     |
|                             | Wear Leveling        |
|                             | Garbage Collection   |



**Figure 5. Sample SoFFS/SoLib Installation**



**Table 3. Points to Remember about NAND Flash Memories and FUJITSU Solutions**

| Points to Remember          |                      | FUJITSU Solutions                                       |
|-----------------------------|----------------------|---|
| Required System Features    | Bad Block Management | SoFFS for NAND  |
|                             | Specific Pin Control | FR30 Control and Connection Reference Simulation Models |
| Recommended System Features | ECC Installation     | ECC Macro   |
|                             | Wear Leveling        | SoFFS for NAND  |
|                             | Garbage Collection   | SoFFS for NAND  |