

Ultra-High-Speed Network Interface Technology for FUJITSU ASIC Devices

New technology, available as an ASIC macro, sends and receives ultra-high-speed data at 2.5 Gbps with clock recovery and enables multiple channel integration with low power consumption of about 150 mW per channel.

Product Overview

The dramatic spread of the Internet and corresponding boom in demand for data bandwidth have led to increased demand for ultra-high-speed interfaces. (Bandwidth is the data rate per channel times number of the channels.) Routers and switches, in particular, require ultra-high speeds and many signal lines to handle terabit (10^{12} bit) and even petabit (10^{15} bit) loads.

As data bandwidth grows, it becomes extremely difficult to handle data at low frequencies. For example, there is a great difference between requirements for handling 160 Gbps with one chip at a frequency of 156 Mbps than at a frequency of 2.5 Gbps.

Data Handling at 156 Mbps

- 160 Gbps/156 Mbps = 1,024
 - 1,024 channels x 2 (for input and output) = 2,048 lines (single end)
- 2,048 signal lines are required at 156 Mbps. With the necessary control signal lines and power lines, this would result in a package size of some 3,000 to 3,500 pins, which would be unrealistic from a cost standpoint. Power consumption would be substantial, and the total system cost would be considerably increased. Also, such a chip would be unable to handle further increases in data bandwidth.

Data Handling at 2.5 Gbps

- 160 Gbps/2.5 Gbps = 64
- 64 channels x 2 (for input and output) x 2 (differential) = 256 lines

At 2.5 Gbps, 256 signal lines are required. Control signal lines and power lines are also required, but a 1,000-pin package is easily sufficient and allows plenty of potential for handling further increases in data bandwidth.

Ultra-high-speed ASSPs capable of handling smaller numbers of channels have already appeared on

“... can be placed in ASICs to allow one-chip integration of many channels ...”

the market, but are not capable of handling the pin count and power consumption requirements of higher numbers of channels.

New FUJITSU technology now provides macros with low power consumption that can be placed in ASICs to allow one-chip integration of many channels for greatly enhanced system data width.

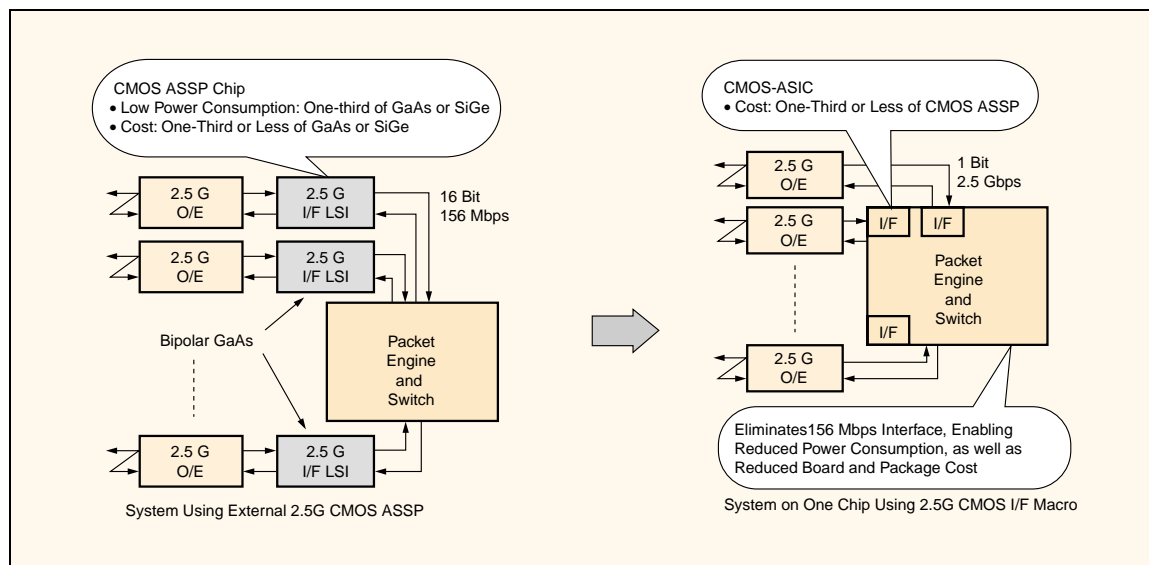
Figure 1 shows the advantages of a CMOS ultra-high-speed interface.

Product Features

- 622 Mbps, 1.25 Gbps, 2.5 Gbps-compatible (on the same macro, programmable)
- Single external clock (reference clock)

- 40 Gbps per macro (2.5 Gbps x 16 channels) (Even higher data rates can be handled by using multiple macros.)
- Built-in CDR¹
- PCML-level differential signals
- Back plane, copper cable, optical module
- SONET² capability scheduled
- 2/4/8/16 channel macros, with 150 mW power consumption per channel (sending/receiving, at 2.5 Gbps); unused channels can be independently switched off
- 1:16 SERDES³ (1:10 for 8B/10B is scheduled.)
- Built-in 50Ω termination resistor (both receiver and transmitter)
- Self testing with loopback (built-in PRBS⁴ generator/comparator)
- 1.8V and 3.3V power supply voltages
- 0.18 μm CMOS (CS80A) technology
- Compatible with standard ASIC design flows
- Verilog/VHDL and Synopsys DC library

Figure 1. Advantages of the CMOS Ultra-High-Speed Interface



Macro Functions

The transceiver (sending/receiving) macros were developed for use in ASIC devices and enable point-to-point data transmission at ultra-high speeds. The transmission paths may be printed circuits, copper wire, or optical modules.

The macro can handle data serialization, parallelization, or clock/data recovery. Data bandwidth expansion within the same system also is possible.

Figure 2 and Figure 3 show a 2.5 Gbps serial interface and parallel interface.

At present, the macro provides 1:16 SERDES; a version with 1:10 SERDES for 8B/10B coding is in development.

This product provides low power consumption of approximately 150 mW per channel, enabling multiple-channel integration (64-channel, 7-Mgate ASICs are currently being

developed). LSI costs and board costs are much lower than for systems using many ASSPs. In

addition, chips are provided with built-in self-testing circuits, enabling at-speed loop-back testing in mass-production chip testing.

Figure 4 (see p. 14) and Figure 5 (see p. 14) show actual measurement results.

“... low power consumption of approximately 150 mW per channel, enabling multiple-channel integration ...”

Figure 2. 2.5 Gbps Serial Interface

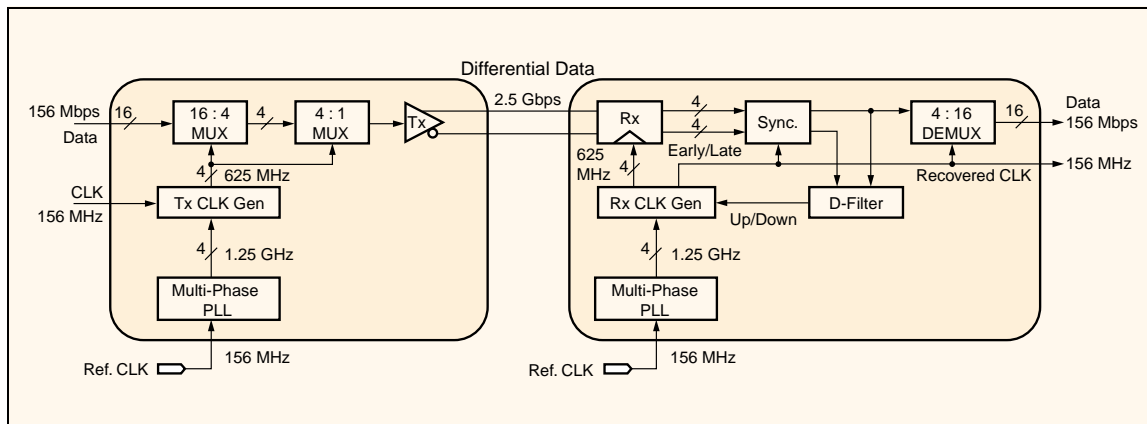
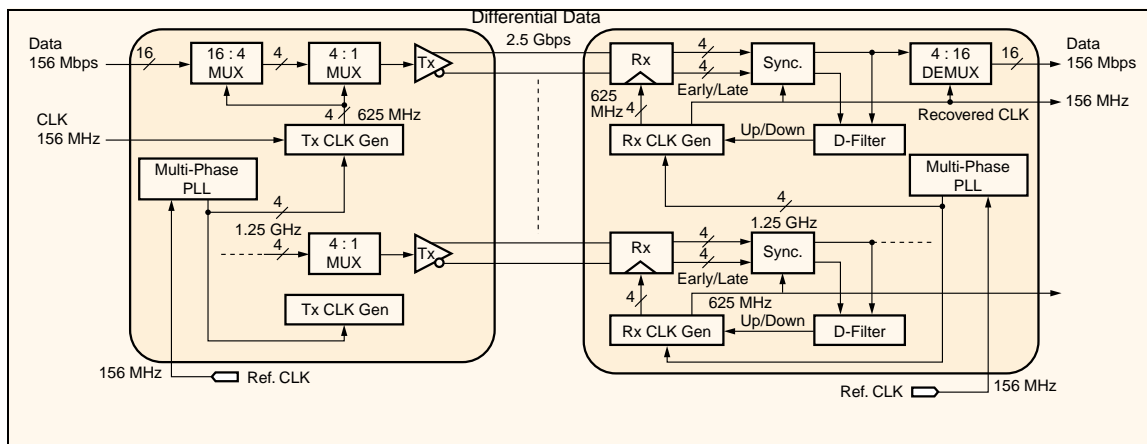


Figure 3. 2.5 Gbps Parallel Interface



Future Development

In the future, FUJITSU plans to add enhanced functions, such as the following:

- Source synchronous: 2.5 Gbps to 3.125 Gbps (OIF SFI-5 compliant)
- 0.11 μm (2.5 Gbps to 3.125 Gbps) CDR and source synchronous
- Much higher data rates: 5/6.4/10/12.8 Gbps, at 0.11 μm (see Figure 6 on p. 15) ♦

Endnotes

- ¹ CDR (Clock data recovery): Recovery of data and clock from a single signal. It eliminates the need to send clock signals separately, used in sending serial signals.
- ² SONET (Synchronous optical network): A standard for synchronous optical communications.
- ³ SERDES (Serializer deserializer): Serialization and deserialization of high-frequency serial data into low-frequency parallel data.
- ⁴ PRES (Pseudo random bit stream/binary sequence): A generator/comparator circuit that generates a pseudo-random signal to verify high-frequency signal operation.

Figure 4. 2.5 Gbps Transceiver Eye Pattern

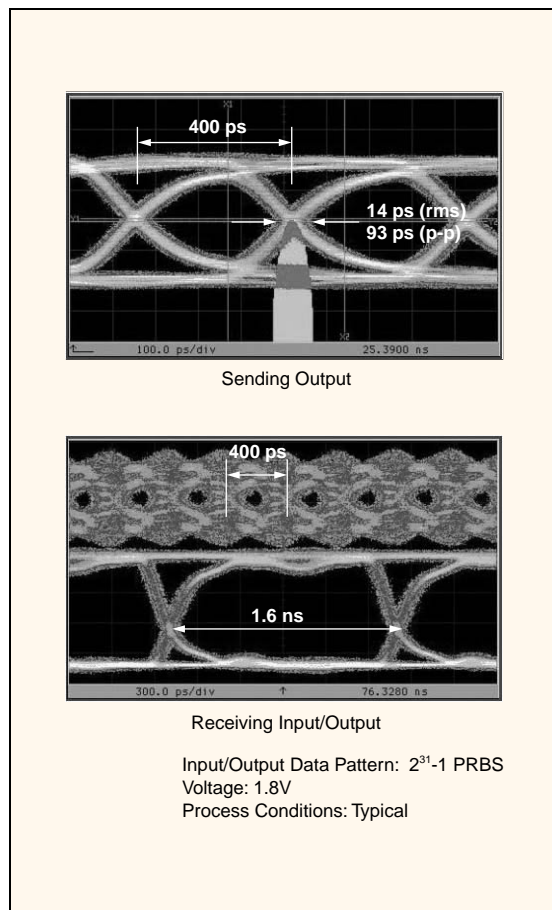


Figure 5. PLL Characteristics

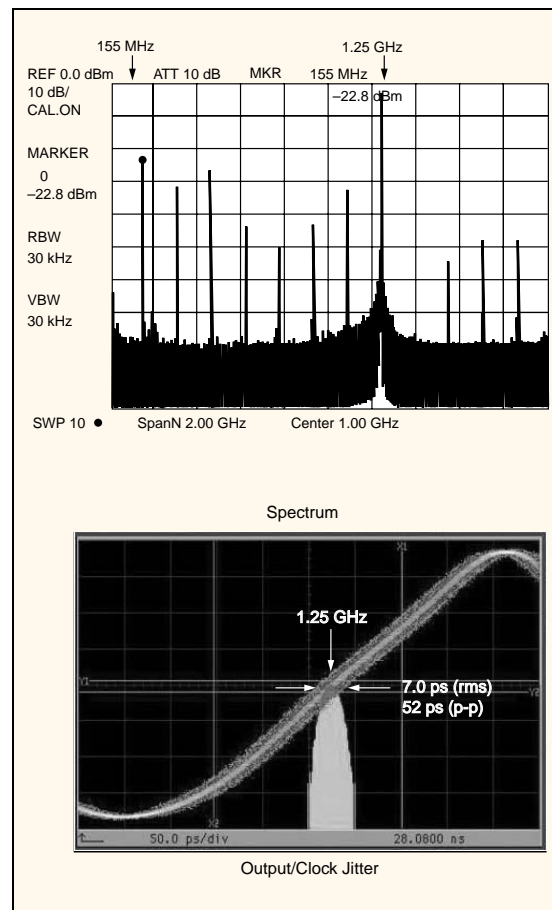


Figure 6. Data Rates and Device Technology Trends

