Flash Memory Solution

FUJITSU provides a high level of support for its flash memory, including SoFFS, SoLib, simulation models, ECC macros, and NAND flash memory control and connection reference resources.

Features

- ***Sophisticated Flash File System (SoFFS)***
- ***Multi-drive support***
- ***SoFFS FAT Access Library (SoLib)***
- ***Simulation***
- ***Solutions for NAND flash memories***
- ***ECC macro***
- ***SoFFS for NAND***
- ***NAND flash memory control and connection reference***
- ***NAND flash memory simulation models***

Introduction

FUJITSU not only develops and offers flash memory devices, but also strives to provide solutions that encompass the software, tools, environments, information, and services that enable our customers to use flash memories with ease. In doing this, we are aiming to establish a “non-volatile memory service business” to respond to all the needs of our clients using flash memory.

In this article we introduce a number of resources for use with flash memory available at FUJITSU.

SoFFS

FUJITSU has developed and marketed Sophisticated Flash File System (SoFFS) software for purposes such as reducing the size of flash memory write units and managing write/erase timing.

By using SoFFS, clients can specify small size units (minimum 128 bytes) for writing into flash memory from operating systems or applications. Erase operations before rewriting can also be eliminated. Functions such as garbage collection and wear leveling, can be used to shorten sector erase time and extend erase cycles for the purpose of emulating operating systems or applications.

SoFFS provides the following functions:

- EEPROM-like operation
- High-speed access
- Data writing uniformity by wear leveling
- Background erase/garbage collection to eliminate wait time
- Low memory use
- Varieties of error detection functions
- Complete data protection functions upon power interruption

Already in use by both domestic and international FUJITSU clients, SoFFS has made major contributions to diversification, reduction, and efficiency in system functions as well as overall system development time and cost reductions.

Multi-Drive Support

Previous versions of SoFFS was set to control only one area of flash memory. When using a two-bank dual-operation flash memory (4 M-bit to 32 M-bit), reading SoFFS codes and application had to be from Bank 1; SoFFS was responsible for writing in whole or in part to Bank 2.

However the 64 M-bit dual-operation flash memory (MBM29DL640) constitutes of four-bank configuration where it makes possible, for example, for a system to erase/write to a sector in Bank 1 while reading data from a consecutive series of bank addresses in Bank 2, followed by Bank 3, and then Bank 4. Or you could virtually allocate physically distant addresses, both Bank 2 and Bank 4, to form one common address space.

Recently significant number of applications and volumes of data handled by our customers' products has grown to become more difficult for systems to manage all data. Instead it is easier to partition systems using the drive concept and control each drive individually.

To accommodate this trend, SoFFS introduces the "drive" as the topmost concept for managing data in flash memory, and includes added multi-drive support functions to manage systems with more than one drive.

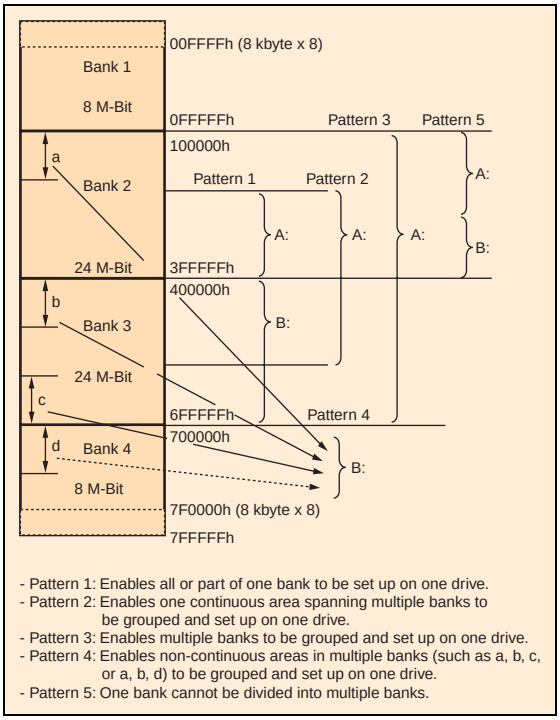
This function provides the following features:

- Introduces the concept of drives
- Capable of reading from other drives while writing is in progress (example: reading from the B: and C: drives during write access to the A: drive)
- Can assign multiple banks to the same drive
- Can assign non-continuous physical addresses within one drive
- Non-exclusive control of access to flash memory
- No read-while-write within the same drive
- No multiple drive partitions within the same bank
- No reflection of physical four-bank configuration in logical drive configuration

Figure 1 shows a conceptual diagram of multi-drive settings.

This new function enables more complex operations and configurations of memory space, as described above.

Figure 1. Conceptual Diagram of Multi-drive Settings



- Pattern 1: Enables all or part of one bank to be set up on one drive.
- Pattern 2: Enables one continuous area spanning multiple banks to be grouped and set up on one drive.
- Pattern 3: Enables multiple banks to be grouped and set up on one drive.
- Pattern 4: Enables non-continuous areas in multiple banks (such as a, b, c, or a, b, d) to be grouped and set up on one drive.
- Pattern 5: One bank cannot be divided into multiple banks.

SoLib

Previously SoFFS allowed applications to control data in terms of virtual block units, simply by specifying the virtual block number of the data to be accessed. This type of interface, however, is not adequate for the multi-function, high-performance products now being developed by our clients, which require access by file units. For this reason we have created a new file access library, SoLib: SoFFS FAT Access Library, positioned above SoFFS. Applications can interface with this library for read/write access to the FAT file system. SoLib can interchange data with external systems such as PCs without difficulty.

Figure 2 shows the positioning of SoLib. SoFFS provides the same interface to access flash memories as previous versions so that all previous SoFFS functions are maintained.

Simulation

As systems become more complicated, with faster speeds, many more functions, and larger capacities, system designers have come to rely on Hardware Description Language (HDL). Flash memories likewise have become more complicated, with faster speeds and multiple function operation.

FUJITSU provides Verilog-HDL/VHDL simulation modeling for use in verifying flash memory operations and checking system design. The simulation models created by FUJITSU have been for the purpose of operation verification, including system design, and therefore are created at the behavior level (operating level) based on datasheets.

Figure 3 shows an example of development processes in system design using simulation modeling.

FUJITSU continues to provide Verilog-HDL/VHDL models for all types of product lines of flash memories.

We also support modeling using the Memory Modeler™ of Denali Software in the United States. Denali models can enhance the simulation performance of Verilog-HDL/VHDL, with features such as using its independently developed language to reduce the amount of memory required during execution. These models can be downloaded from the FUJITSU Web page.

Figure 2. Positioning of SoLib

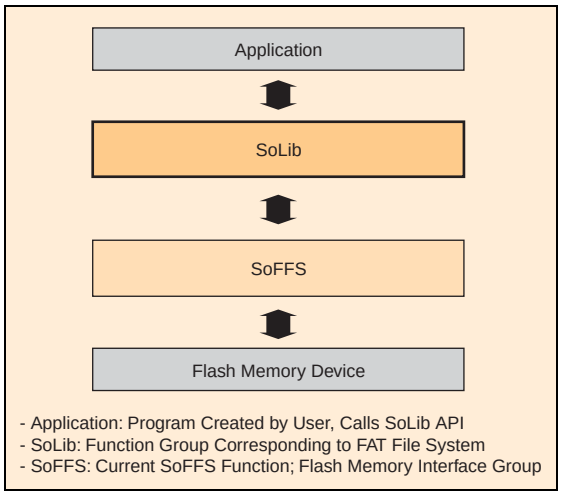
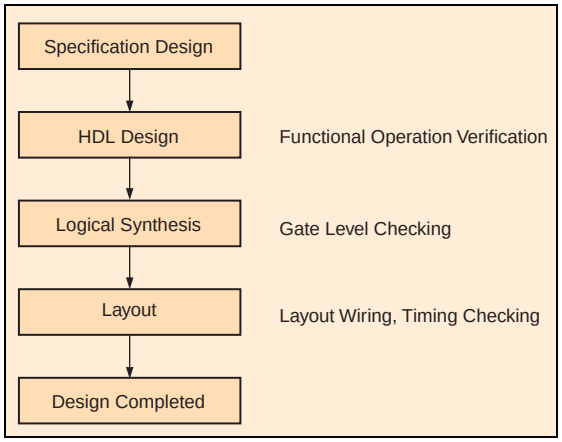


Figure 3. Example of Development Processes in System Design



Solutions for NAND Flash Memories

The rapid growth of portable devices has led to increasing demand for compact, high-capacity memory media for data storage. To respond to this demand, FUJITSU is developing and supplying NAND flash memory products, which are more easily adapted to large capacities and better suited for data storage than NOR flash memories.

Figure 4 shows a roadmap of FUJITSU NAND flash memory development.

Table 1 shows a comparison of the NAND flash memory and NOR flash memory in terms of read/write/erase times. The comparison shows that NAND flash memories have faster write/erase times than NOR memories and are better suited for high-volume data storage.

Figure 5 (see p. 38) shows the direction of flash memory demand for standard uses.

FUJITSU is emphasizing not only the production of flash memories themselves, but also providing total solutions, including software, tools, and information for building memories more efficiently and promptly into our clients' products.

The remainder of this article introduces solutions for NAND flash memories.

Figure 4. NAND Flash Memory Road Map

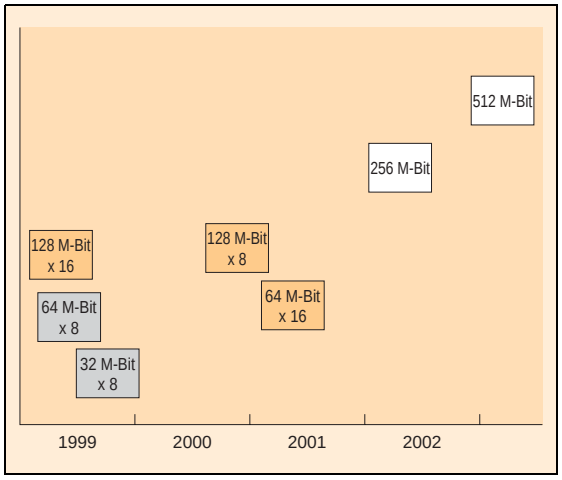


Table 1. Comparison of NAND Flash Memory and NOR Flash Memory

Parameter	NAND Flash Memory*	NOR Flash Memory
Read Unit	Page (512 + 16 bytes)	Byte / Word
Access Time (typ.)	7µs (initial access), 50ns (serial access)	90ns (random access)
Write Unit	Page (512 + 16 bytes)	Byte / Word
Write Time (typ.)	200µs	8µs/byte 16µs/word (4ms/528 bytes)
Erase Unit	Block (8K + 256 bytes)	Sector (8K/64Kbytes)
Erase Time (typ.)	2ms	1s

* Using MBM30LV0064

ECC Macro

Error Correcting Code (ECC) macro for 1-bit error correction and 2-bit error detection is provided in the form of Verilog, VHDL, and C. It is a type of humming code, and is characterized by the fact that only 3 bytes of ECC code is generated per one page (512 bytes). This macro can be built into hardware macro on ASIC circuit in client products.

Figure 6 (see p. 38) shows an example of the placement of an ECC macro. Specifically, the following are available.

- ECC macro source code (Verilog, VHDL, C)
- ECC macro specification document
- ECC macro application note

SoFFS for NAND

FUJITSU, already providing SoFFS software for NOR flash memories, has now developed SoFFS for use with NAND memories. The new product is called SoFFS for NAND, and provides the following functions:

- Wear leveling
- Garbage collection
- Management of bad blocks

In addition, the SoLib access library is available for FAT interchangeable file systems.

Figure 7 (see p. 38) shows an example of SoFFS and SoLib installation. Specifically, the following are available:

- SoFFS for NAND source code
- SoFFS for NAND manual
- SoFFS for NAND descriptive documents
- SoLib for NAND object code
- SoLib for NAND specification

NAND Flash Memory Control and Connection Reference

Sample connections and circuit diagrams for connections to the FUJITSU FR30 Series of 32-bit RISC microcontrollers are available as reference material for CLE, ALE, and SE pin control and connections. In these examples, registers control these special pins. Specifically, the following are provided:

- Sample specifications for connections between FR30 and NAND flash memory
- Sample circuit diagrams for connections between FR30 and NAND flash memory
- NAND flash memory expansion board for FR30 evaluation board use (available by lease only)

NAND Flash Memory Simulation Models

At present, VHDL, Verilog, IBIS, and Denali models are available for use with 64 M-bit MBM30LV0064 products.

Table 2 (see p. 38) shows the challenges to users of NAND flash memories together with the corresponding FUJITSU solutions.

Future Development

FUJITSU will be adapting each of these solutions to all of our future flash memory products. In addition, we plan to serve our clients as a provider not only of the flash memory devices themselves, but also of a wide variety of solutions and services including software, tools, models, and information related to the use of flash memory.

Figure 5. Flash Memory Use by Objective

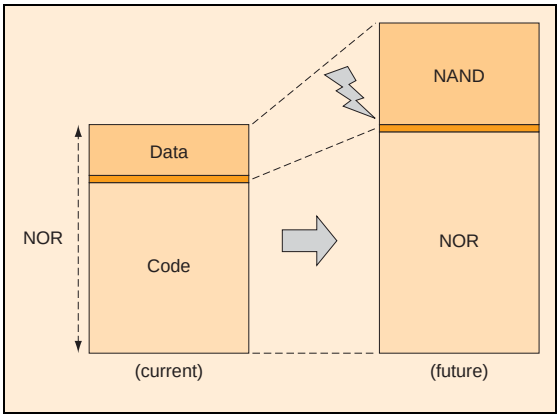


Figure 6. ECC Macro (Example)

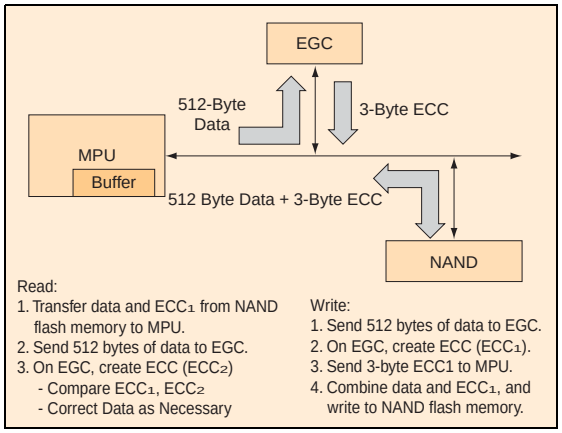


Figure 7. SoFFS/SoLib Installation (Example)

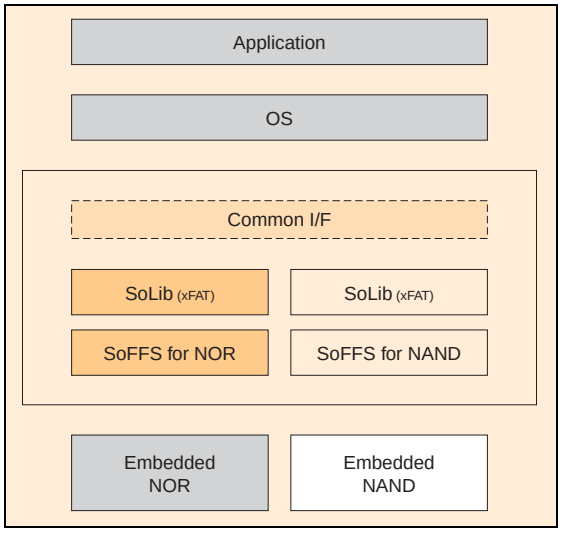


Table 2. NAND Flash Memory Issues and FUJITSU Solutions

Issues for Concern		FUJITSU Solution
Issues that must be addressed	Invalid Block Control	SoFFS for NAND
	Exclusive Pin Control	Simulation Model, Reference for Control and Connection to FR30 Core
Issues that should be addressed	ECC Installation	ECC Macro
	Wear Leveling	SoFFS for NAND
	Garbage Collection	SoFFS for NAND