

0.11- μm CMOS Standard Cell and Embedded Array: CS91 Series/CE91 Series

The CS91 Series standard cell and CE91 Series embedded array are designed for use in leading-edge networking and communication equipment.

Features

- **High gate count: 48 million**
- **High speed: 16 ps gate delay time (CS91)**
- **Low power consumption: 6.6 nW per gate**
- **High-density BGA packaging**
- **IP macro support**

Overview

This article describes the newly developed CS91 Series 0.11- μm ASIC standard cell and CE91 Series embedded array. These products were developed for applications in leading-edge networking and communications equipment, where the require-

ments are for high pin counts and fast transmission speeds. They are also a good fit in mobile equipment that requires a wide range of functionality and low power consumption. The products feature high pin-count packages, high-speed interfaces, and high-speed/low-leak cell libraries.

Product Features

Higher Speed, Higher Integration

Technologies incorporated in these devices include 0.11- μm gate length transistors, eight-layer ultra-fine pitch for miniaturization and reduced influence on electrical characteristics, copper wiring, and low-K inter-layer material¹ ($k \leq 2.6$). By improving the power supply delivery to the entire chip and to the macro peripherals, the devices now contain more than 48 million gates (CS91, full coverage).

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The 16 picosecond gate delay time (CS91, high-speed library, inverter, 1.2V operation) is approximately 50% faster than that of products using the conventional 0.18 micron technology.

The product range includes embedded arrays (CE91) that have an established reputation for ease of design and for shorter turnaround time to fabricate engineering samples. The maximum chip frame is able to contain 38 million gates (full coverage).

IP Macros

To simplify the implementation of sophisticated system LSIs, the products support a range of standard operational macros, including CPU macros, various peripheral macros, memories, adders, and multipliers, as well as PLLs, analog macros, and high-speed I/F macros.

Table 1 (see p. 51) lists the supported IP macros.

Design Procedure

A hierarchical design methodology, timing-driven layout, and crosstalk suppression layout/modification are used to deal with large circuit sizes, timing problems, and signal integrity problems. These can be performed automatically as part of the SCCAD (CS91) and GLOSCAD (CE91) design process.

Low Power Consumption, Low Voltage Operation, Low-Leak Current

The devices can operate at the standard 1.2V \pm 0.1V power supply down to a minimum of 0.8V. Power consumption has been reduced to 6.6 nW (power

consumption per gate for the CS91 at 1 MHz and fanout = 1), approximately half the power consumption of the previous generation of 1.2V devices. A special, low-leak current cell library is provided for the mobile equipment market where reduced standby power consumption is required.

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Testing Procedures

The MUX-D methodology, which has been successfully used in previous product series, supports path delay tests for scan and real-time operation verification. In addition, logic BIST² is supported for verifying operation at high speed that cannot be measured using an LSI tester.

Packages

FUJITSU has developed high pin-count packages and fine-pitch solder bump technology for the chips to meet the demand in the networking market for high pin counts and high transmission speeds. Packages currently used in existing product series can also be selected, simplifying the development of replacements for existing products.

The following packages are available, including packages not yet released:

- FCBGA package: 2,116 pins max.
- EBGA package: 672 pins max.
- FBGA package: 304 pins max.
- TAB-BGA package: 720 pins max.
- QFP package: 304 pins max.

Table 2 lists the specifications, Table 3 (see p. 52) lists the maximum ratings, and Table 4 (see p. 52) lists the recommended operating conditions. Table 5 (see p. 52) lists the DC characteristics, and Table 6 (see p. 53) lists the development support tools. ◆

Endnotes

¹ Low-K inter-layer material: Inter-layer material that has low permittivity

² BIST: Built-In Self Test

Table 1. Supported IP Macros

CPU/DSP	ARM9, ARM7TDMI, and Others Communication DSPs, Digital AV DSPs, and Others
Interface Macros	PCI, IEEE1394, USB, IrDA, and Others
Multimedia Macros	JPEG, MPEG, and Others
Mixed Signal Macros	ADC, DAC, OPAMP, and Others
Compiled Macros	RAM (1-port, 2-port), ROM, Multiplier, Adder, AND/OR Logic
PLL	Analog PLL, Digital PLL
I/O Macros	LVDS, T-LVTTL, P-CML, PCI, SSTL2, HSTL, GTL, AGP, USB, IEEE1394, and Others
High-Speed I/F Macros	622Mbps I/F, 2.5Gbps I/F, 3.2Gbps I/F, 10Gbps I/F

(includes macros under development)

Table 2. CS91 Series and CE91 Series Specifications

Series Name		Standard Cell CS91	Embedded Array CE91
Part No.		MB87QXXXX (last 4 characters are specified by FUJITSU)	
Process Technology		0.11- μ m Si Gate CMOS, 5 to 8 Layer Wiring (using Cu), Low-K Inter-Layer Material	
Gate Count		48,000,000 or more Gates	38,000,000 Gates
Electrical Performance	Delay Time* ¹	16ps	20ps
	Power Consumption* ¹	6.6nW/MHz	10.4nW/MHz
	Interface Level	2.5V* ² 3.3V* ³	

*¹ Inverter Cell, Fanout = 1

*² Available when 2.5V is supplied as I/O power supply.

*³ Available when 3.3V is supplied as I/O power supply.

Table 3. Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit
Power Supply Voltage	VDD	3.3V Power Supply (I/O)	-0.5 to 4.6	V
		1.2V Power Supply (internal)	-0.5 to 1.5	
Input Voltage	VI	3.3V Power Supply	-0.5 to VDD + 0.5 (≤ 4.0)	
Output Voltage	VO	3.3V Power Supply	-0.5 to VDD + 0.5 (≤ 4.0)	
Storage Temperature	Tstg	—	-55 to +125 (plastic)	°C

Table 4. Recommended Operating ConditionsVDDI=1.2V \pm 0.1V, VDDE=3.3V \pm 0.3V (dual power supply)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	VDDI	1.1	1.2	1.3	V
	VDDE	3.0	3.3	3.6	
"H" Level Input Voltage	VIH	2.0	—	VDDE + 0.3	
"L" Level Input Voltage	VIL	-0.3		0.8	
Operating Junction Temperature	Tj	-40		125	°C

Table 5. DC CharacteristicsVDDI=1.2V \pm 0.1V, VDDE=3.3V \pm 0.3V (dual power supply)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
"H" Level Output Voltage	VOH	IOH=-100 μ A	VDDE-0.2	—	VDDE	V
"L" Level Output Voltage	VOL	IOL=100 μ A	0		0.2	
"H" Level Output Current	IOH	L Type, VOH=VDDE-0.4V	—		TBD	mA
		M Type, VOH=VDDE-0.4V			TBD	
		H Type, VOH=VDDE-0.4V			TBD	
"L" Level Output Current	IOL	L Type, VOL=0.4V	TBD		—	—
		M Type, VOL=0.4V	TBD			
		H Type, VOL=0.4V	TBD			
Input Leak	IL	—	-10		10	μ A
Pull-Up Resistor	Rpu	VI=0	—		33	—
Pull-Down Resistor	Rpd	VI=VDDE	—	33		

* Values are subject to change.

Table 6. Development Support Tools

Function	Tool Name
Logic Synthesis	"DesignCompiler" and "Physical Compiler" from Synopsys "BuildGates" from Cadence
Power Calculation	"Watt Watcher" from Sequence (available on request) "DesignPower" and "PowerCompiler" from Synopsys "PowerImpuls" from FUJITSU
Timing Analysis	"PrimeTime" from Synopsys "Gista" from FUJITSU
Simulation	"Verilog-XL", "NC-Verilog" and "Leapfrog" from Cadence "VSS" and "VCS" from Synopsys "Model-sim" from Model Technology "LCADFE" from FUJITSU
Formal Verification	"Design VERIFYer" from Avant! "Formality" from Synopsys "Tuxedo-LEC" from Verplex "Assure" from FUJITSU
Layout	"Blast Fusion" from Magma "Integrated Ensemble" from Cadence "SCCAD", "GLOSCAD" from FUJITSU
Test Tools	"icBIST" from Logic Vision "ATREX", "FANTCAD", "RAPARA", "TERBAN", and "FANSCAD" from FUJITSU
Verification Tools	"Assura" from Cadence "Calibre" from Mentor
HW/SW Co-Simulation	"EAGLE-i" from Synopsys "VIRTUAL-ICE" from Yokogawa "Asim-G" from GIAO Technology