Image-Processing LSIs for Cellular Phones

MB86V00/MB86V01

MB86V00 and MB86V01 are single-chip, low-power-consumption LSIs that incorporate high-resolution camera/video functionalities best suited for cellular phones and other mobile equipment. These devices incorporate ARM7TDMI™ and provide hardware support for multimedia processing.

Product Description

Today's cellular phones are widely used not only as simple devices to make telephone calls, but also as multimedia tools that offer digital still camera, digital camcorder, and/or gaming functionalities; this reflects the market demand for more characteristic and higher quality photographic and video contents. In fact, cellular phones incorporating camera modules are increasingly spreading not only in Japan, but also in the world market including Europe and America and even China where remarkably high economic growth has been achieved in recent years.

FUJITSU has now developed LSIs oriented for the world market that implement high-resolution camera/video functionalities on a single chip with lower power consumption. These are expected to be essential requirements for cellular phones and other mobile equipment in the future.

System

The new devices incorporate ARM7TDMI 32-bit RISC processor (simply called ARM7 hereinafter). The devices may be connected with baseband chips which process transmission in the cellular phone systems to capture still shots or encode/decode video-stream data. They incorporate 2D/3D graphics engines that allow the superimposing of 2D/3D animations on the captured contents (superimpose function) or the capturing of superimposed images as still or video pictures. Thus the new devices act as image-processing LSIs that are chiefly intended for multimedia processing. Generally, baseband chips are required to manage and control the individual modules for image-processing LSIs, though the new devices relieve the baseband chips from the heavy loads of multimedia data processing owing to the built-in ARM7. Even in systems configured with relatively low-throughput baseband chips, advanced multimedia processing can be achieved by connecting

Photo 1 External View

with these new devices.

The new devices also provide hardware support for almost all of the functions required for multimedia processing. For cellular phone systems, lower power consumption and extended standby time constitute essential requirements. In the systems using the new devices that provide hardware support for multimedia processing, the benefit of considerably reduced power consumption is obtained compared to systems that use processors and/or DSP for software processing. In addition, when the need arises for the incorporation of additional features into a system, the new devices can achieve it using the built-in ARM7 without making any changes to the system.

FUJITSU offers two types of LSIs to meet customer-specific application needs: one is MB86V00, which integrates 64M-bit SDRAM with logic chip as a one package (SIP), the other is MB86V01 without integrated SDRAM.

Product Features

Table 1 lists the principal specifications and available functions, and **Fig.1** presents an internal block diagram.

ARM7TDMI

The new devices incorporate the ARM7TDMI, which contains an 8Kbytes cache operating on a maximum frequency of 54MHz. The devices also incorporate 16Kbytes SRAM.

MPEG-4 hardware encoding/decoding

The new devices support the encoding and decoding of video-stream data in the format of MPEG-4 Ver.1, simple profile. All of the processing capabilities required for video-stream configuration/analysis are installed in the hardware to offer low power consumption and high-performance features. Encoding or decoding can be processed at a maximum speed of 30fps for CIF, 15fps for QVGA (video-conferencing, etc.), and 15fps for VGA[*1].

Error-correcting processing by RVLC reverse-direction searching is also supported to allow optimum codec function even in an environment of extremely lower error resistance.

JPEG hardware codec

The new devices contain the user-definable Huffman Table (2 tables each for AC and DC) and Quantization Table (4 tables) to support the compression/decompression mode of JPEG baseline format. They support YUV4.2.2, 4.1.1, and 4.2.0 data formats. They can compress 2 MPixels (1,600×1,200) data at approximately 2.2 frames per second.

Camera module interface

The new devices can capture YUV4.2.2-format image data in synchronization with any externally supplied clock. The devices accommodate input clocks of up to 48MHz, and display maximum VGA resolution 1,616×1,236 pixels of 2MPixels (1,600×1,200) data on the preview screen at 10 to 12fps. Data may be reduced to any size (resolution) while it is being captured. The new devices incorporate an LPF (low-pass filter) with 5-tap in the horizontal and 3-tap in the vertical. In addition, in the process of image capturing, frame data may be thinned out.

2D/3D graphics

The new devices incorporate functions for the processing of Gouraud shading, Z buffering, and other techniques for three-dimensional (3D) rendering, alpha blending, texture mapping, and anti-aliasing for smooth line drawing[*2].

Table 1 Principal Specifications and Available Functions

Internal operating frequency	54MHz (External supply clock frequency 13.5MHz, SDRAM 108MHz)
Operating voltage	Core voltage : 1.8±0.15V External I/O : 2.6 - 3.6V
Technology	Low-Leakage 0.18 μm CMOS technology
Package	FBGA 289 pins (Size: 10 mm×10 mm)
Main functions	・ARM7TDMI (54MHz) cache incorporated ・MPEG-4/JPEG hardware codec engine ・Camera interface supporting 2 MPixels ・2D/3D graphic controller ・LCD controller compatible with CPU I/F ・Format converter, scaler, rotation ・ITU-R BT.656-compliant 8-bit interface ・Other peripherals (I²C, timer, UART, GPIO, PWM, etc.) ・SRAM slave I/F type Host-CPU interface

LCD interface

The new devices can interface with the LCD modules of maximum 16,777,216-colors VGA-size CPU-I/F type, and 8/16/18/24-bit bus width configuration*3 to provide support for two-screen superimposing, alpha-blending, transparency, partial displaying, and other functions. The devices may be applied to systems containing two LCDs (sub and main) by incorporating the chip selector signals for LCDs. In addition, direct access to the built-in SRAM in the LCD module from the host CPU is also available. Direct access to the LCD is attained at approximately 2mA of power consumption. (It is recommended to limit the clock supply to the updating of clock data on the standby screen of cellular phones and to interrupt the clock supply in other cases. In this case, power consumption is reduced to approximately 30μA.)

Format converter, scaler, rotation

The new devices support the conversion of YUV data, a data format used for pictures and video images, and that of RGB-format data used in graphics.

The scaler supports the resolution conversion function from a minimum of 1/16 up to 256 times. Resolution conversion is available with either method, bicubic (4×4 matrix operation) or bilinear (2×2 matrix operation).

Photo 2 Evaluation Board

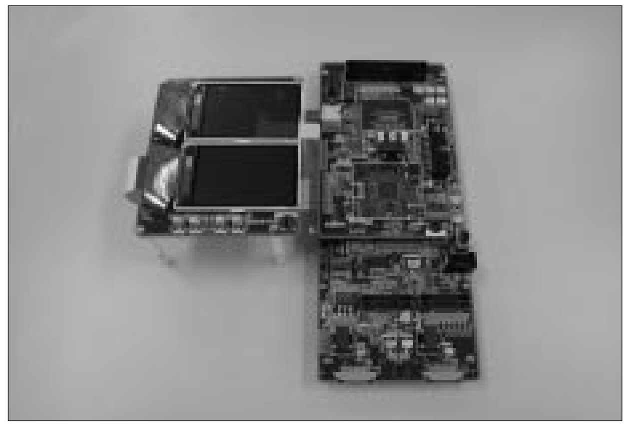
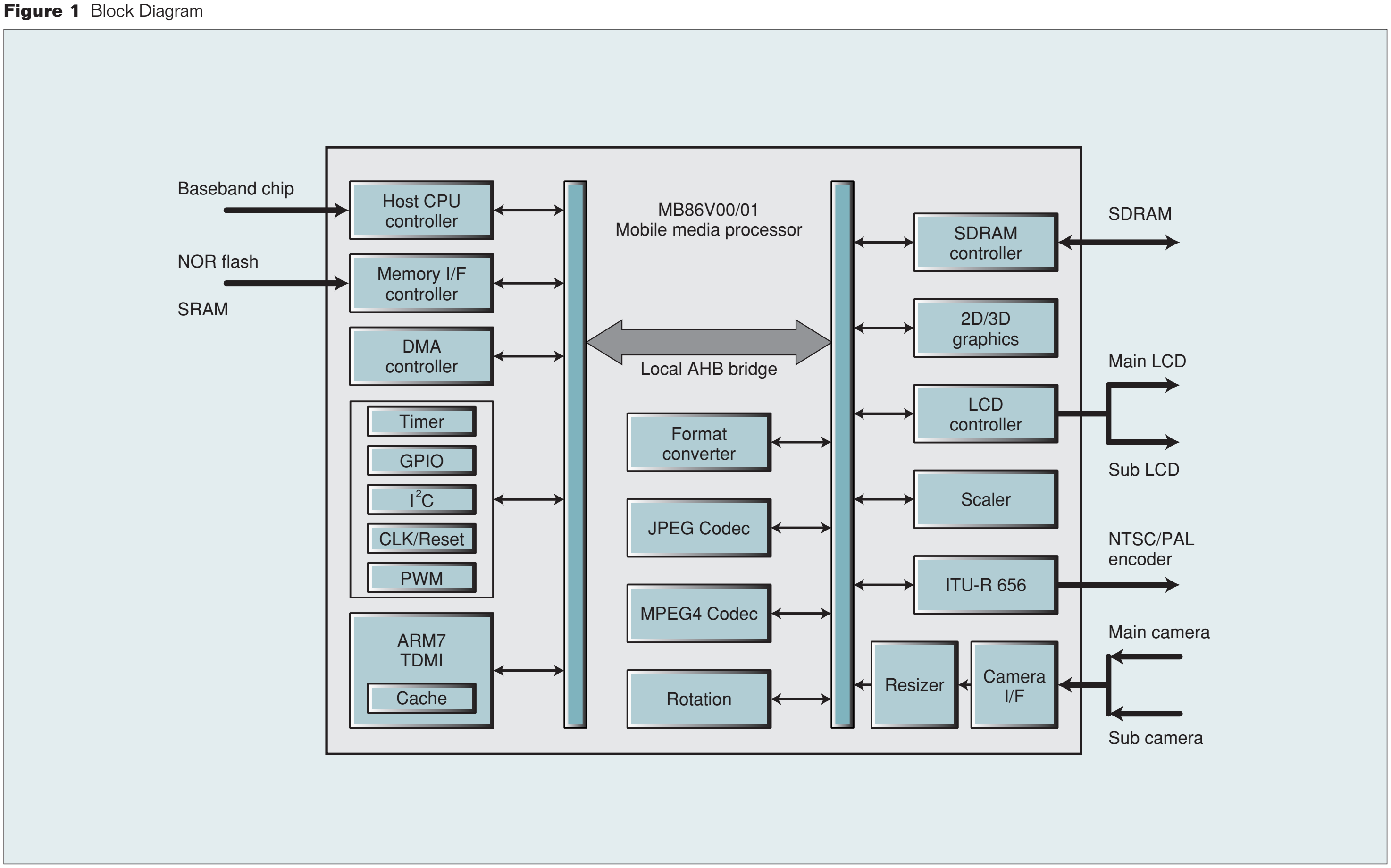


Figure 1 Block Diagram



The rotation function is available for YUV-format data with rotation of images in units of 90 degrees.

■ ITU-R.BT656 8-bit parallel output

ITU-R.BT656-based 8-bit parallel data is output to allow the new devices to display TV images when connected to an NTSC/PAL encoder and DAC.

■ Host CPU interface

Through the SRAM slave I/F-type asynchronous data bus, access from the host CPU to the internal registers in the new devices, transfer of display lists, reading/writing of codec data, and reading from writing into the VRAM (SDRAM) area are available. The host CPU also supports the wide-address mode (address width 19 bits) and the narrow-address mode (address width 8 bits) as indirect-address access.

■ Peripherals

The new devices incorporate I^2C interfaces (standard/high-speed modes) for the control of camera modules and NTSC/PAL encoders. Only the master functions of I^2C are supported. The 16-bit timer, UART, PWM, GPIO, and other peripherals are also supported.

Evaluation and Development Environment

The new devices contain the JTAG I/F and thus allow development based on the ADS and Multi-ICE™ of ARM. For advanced development of software and hardware evaluation, an evaluation board is available. The evaluation board contains a 310,000-pixel (VGA) CMOS camera module, QVGA-size LCD module, 4Mbytes flash ROM, 1Mbytes SRAM, 64M-bit SDRAM (available with MB86V01 only), and NTSC/PAL video encoder chip in addition to the new devices. Development using the host I/F is also possible, in which case the OS-independent software API is available. ✱

NOTES

∗1: VGA-size encoding/decoding formats are not specified in the simple profile. The processing of VGA-size data is based on special specifications intended for the new devices; as such, data compatibility with other products' codec is not guaranteed.

∗2: A geometry engine is not incorporated. For the processing of light sources, a CPU is required.

∗3: The upper 6-bit data [23:18] shares the terminals with GPIO.