

# Introduction of FR400 Series

The FR400 Series is a new cost-effective processor developed by making several modifications to the higher-end FR500 Series. By deleting the floating-point unit, changing the instruction issuing patterns, and enhancing the instruction processing capabilities, FUJITSU has successfully developed a low-profile, high-performance processor with substantial energy-saving features. This series has double or more the cost effectiveness and performance of the FR500 Series.

## Product Description

### Product Features

The most attractive feature of FR400 Series is its low-profile and high-performance core. The chip architecture is based on earlier FR500 Series processor designed for true media processing, but modified in several ways to realize a lower-profile architecture while maintaining downward compatibility.

New series adopts a 2-way VLIW (Very Long Instruction Word) instead of 4-way VLIW employed in FR500 Series, and deletes the floating-point unit. This modification substantially reduces the hardware resources, and improvements in the instruction processing capabilities make the processor at least twice or more as cost-effective as FR500 Series.

The FR400 Series incorporates a media-processing unit capable of carrying out MAC operations for a maximum of four (4) pieces of 16-bit fixed-point data simultaneously. Using the instruction sets within this new media-processing unit, the device can process images, JPEG, and other applications. Moreover, the media processing capabilities are further improved through the installation of additional instruction sets to improve the processing of JPEG/MPEG data.

FR400 Series incorporates a set of integer instructions (including logical operations, load/store instructions, control instruction, and compiler support) together with its media instruction sets, ensuring high performance in system control

and integer system processing.

**Table 1** shows instruction issuing patterns available with FR400.

### Target Market

FR400 Series is targeted chiefly for the markets listed below. The low-profile core and high-performance media processing capabilities of FR400 make it an ideal choice for these markets, all of which demand a versatile range of capabilities for processing images, JPEG, MPEG, and other sophisticated formats.

#### ■ Imaging market

- Multi-function printers (MFP)\*1

**Table 1** FR400 Instruction Issuing Patterns

Slot 0	Slot 1
Integer-0	—
Integer-0	Media-0
Integer-0	Integer-1
Integer-0	Branch
Media-0	—
Media-0	Media-1
Media-0	Branch
Branch	—
Control	—

- Host-based printers\*<sup>2</sup>
- Next-generation home-use printers (Internet printers)
- Image recognition units and security systems

■ **Media processing market**

- Personal digital assistant (PDA)
- Multimedia units\*<sup>3</sup>

**FR-V Family Road Map**

FR-V Family is an extremely wide ranging family of products from low end to the very highest end, designed to process both integers and the countless combinations of media used for instruction sets and data in parallel arrangements.

FR400 Series is a low-profile, easy-to-use media processor designed to issue a maximum of two instructions at once. FR500 is a higher-end sibling of FR400, designed to process up to four instructions simultaneously in order to handle more demanding media-processing applications. FUJITSU has already developed FR550 Series processor capable of issuing a maximum of eight instructions at once. This future chip will be configured with an innovative core that considerably improves upon the instruction issuing and integer processing capabilities of FR500.

FUJITSU is making consistent efforts to develop architectures for the generations to come, as well as also SoC (System on Chip) devices configured with FR-V cores and dedicated to single applications.

FR400 Series is oriented toward:

- SoC configuration: Peripheral circuits and application-specific functions are all packaged in a single chip.
- Higher performance: Performance is enhanced by improving the operating frequency, cache memory, and bus transfer capability.

**Fig.1** provides an FR-V Family Road Map, and **Fig.2** outlines the basic concept of the FR-V SoC.

**Implementation**

MB93401A is the first LSI configured with FR400 core. MB93401A has the features listed below.

- FR400 core is mounted in the same chip in conjunction with DMAC, UART and other peripheral facilities, thereby allowing direct connection to SDRAM and peripheral circuits.

The SDRAM memory bus is separated from the peripheral circuit interface bus, and thus the processing at the core is kept away from any effects even if the peripheral circuits are used at lower speeds.

- The built-in SDRAM is compatible with any SDRAM of up to 256Mbit/PC133 and connects internally to the core via a high-speed bus interface. The internal connection ensures efficient memory access with minimum latency time.
- The operational sequence of the core, SDRAM, and buses may be controlled as necessary with the aid of a clock gear and standby facilities. In addition, configurations with lower power circuits can be used for further energy saving.

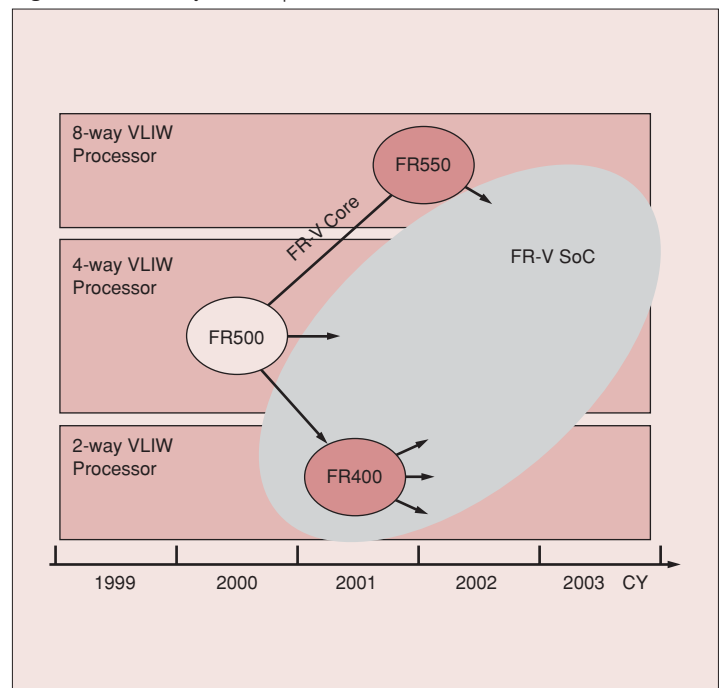
■ **Principal specifications of MB93401**

- Architecture: 2-way VLIW
- Clock: 200/266MHz
- Peak Throughput: 532MIPS at 266MHz, 2394MOPS at 266MHz
- Power Consumption: Core 500mW
- Process: 0.18μm CMOS
- Package: 288FBGA
- Built-in Peripherals: SDRAM I/F (Max. 64bit/133MHz)  
DMAC (4 channels/Circular, with 2D transfer option)  
IRC (External interrupt 4 channels)  
UART (2 channels)  
Timer (3 channels)

**Fig.3** shows a block diagram of MB93401A.

MB93401A provides a throughput of 532MIPS and 2394MOPS. At this level of performance, the LSI can serve as a high-performance processor for system control, and also run

**Figure 1** FR-V Family Road Map



code for any type of processing conventionally carried out by DSP or hardware. Spatial filter, JPEG, MPEG and other media can all be processed, as well as a wide variety of signals.

MB93401A can be incorporated in any product as a general-purpose LSI package, or it can be used as an evaluation chip for feasibility studies of any FR400 core-based SoC. The device incorporates versatile, high-performance buses to allow easy reconfiguration of peripherals with the use of the core alone.

## FR-V Integrated Development Environment

### FR400 Development Environment

FUJITSU's original software development environment SOFTUNE consists of the following elements.

- C/C++ Compiler
- Assembler/Linker/Librarian
- Workbench

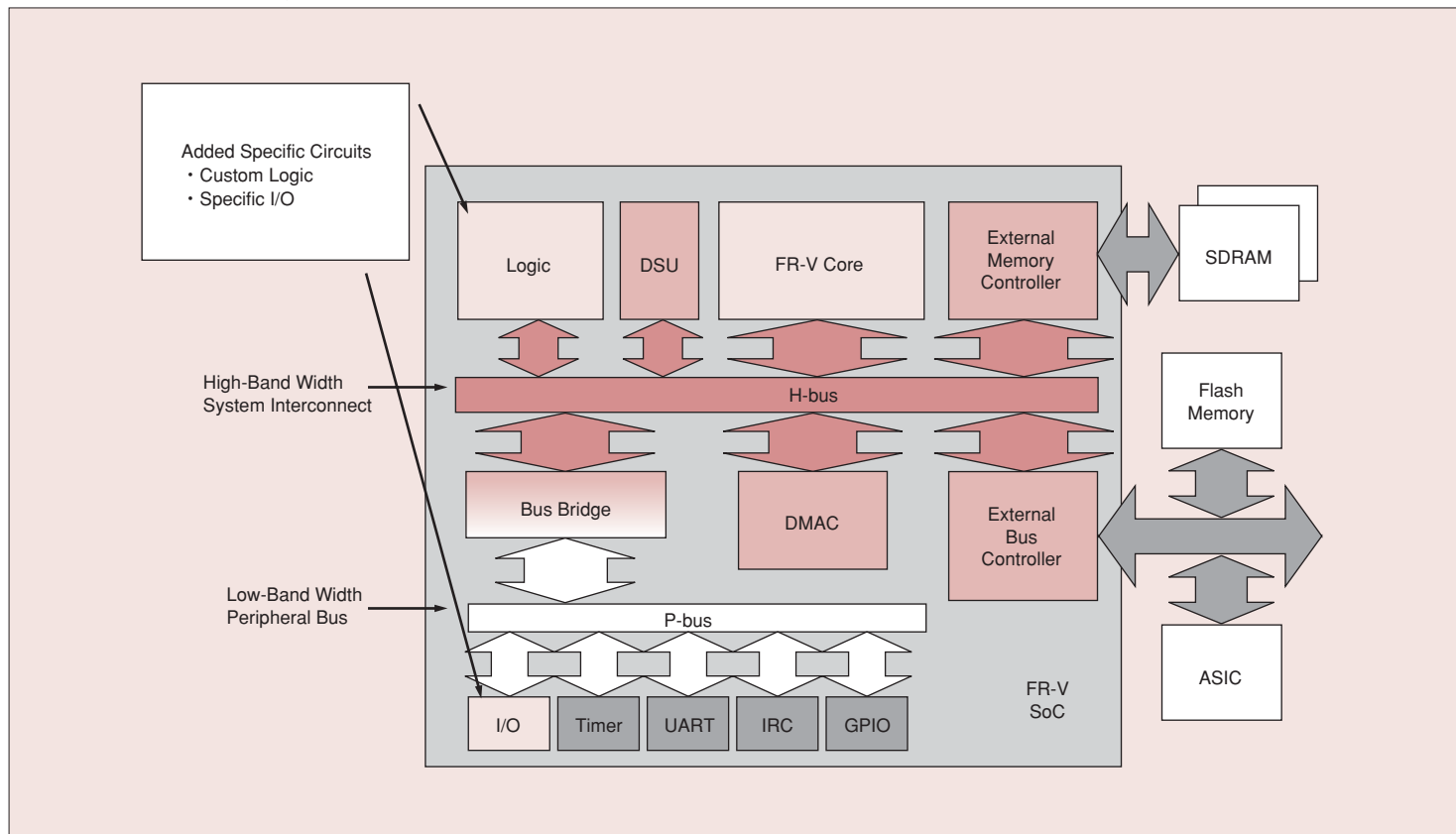
### • Debugger

FUJITSU's based the design of its compilers on the sophisticated VLIW optimization technology continuously refined by the company as it develops more advanced super computers. The program can be optimized by making full use of the compiler support instructions (predicate instructions, etc.) incorporated in FR400.

SOFTUNE integrated development environment requires no special programming ability. Programming and debugging operations are executed simply, in quite the same way within a typical RISC processor. Moreover, SOFTUNE environment integrates the functions of a compiler, OS configuration, debugger, OS analyzer, and other development tool sets, thereby allowing the efficient execution of complete task sequences, from program modification to debugging, within the same environment. It also provides powerful support for the tuning of programs by incorporating a profiler to analyze execution performance.

SOFTUNE can be used with both FR500 and FR400.

Figure 2 FR-V SoC Basic Configuration



**Embedded OS**

■ SOFTUNE™ REALOS™/FRV

SOFTUNE REALOS/FRV is an Realtime OS (kernel) that conforms to the specifications for the latest  $\mu$ ITRON version 4.0 (standard profile), the current industry standard for embedded devices in Japan. This high-speed, compact kernel is coded to deliver maximum performance with the FR-V architecture.

■ Linux

"axLinux" \*4 is now developing to provide an embedded OS Linux optimized for the FR-V architecture. The axLinux has excellent features, a compact size, reliable and easy-to-use network accessibility, and multi-task support optimized for multimedia.

**FUJITSU ICE (MB2199-01, 10)**

FUJITSU's ICE allows break and/or trace options even while running at full speed with the cache enabled. By building the break-detection function into the hardware, it can even debug code stored in ROM. Like the JTAG ICE, this ICE is designed to respond to serial communication signals for connection with the debug support unit (DSU) in FR400 core. It can be

interfaced with a host machine via RS232C or USB. The ICE can be used with both FR500 and FR400.

**FR-V Design Kit (VDK: FR-V Design Kit) \*5**

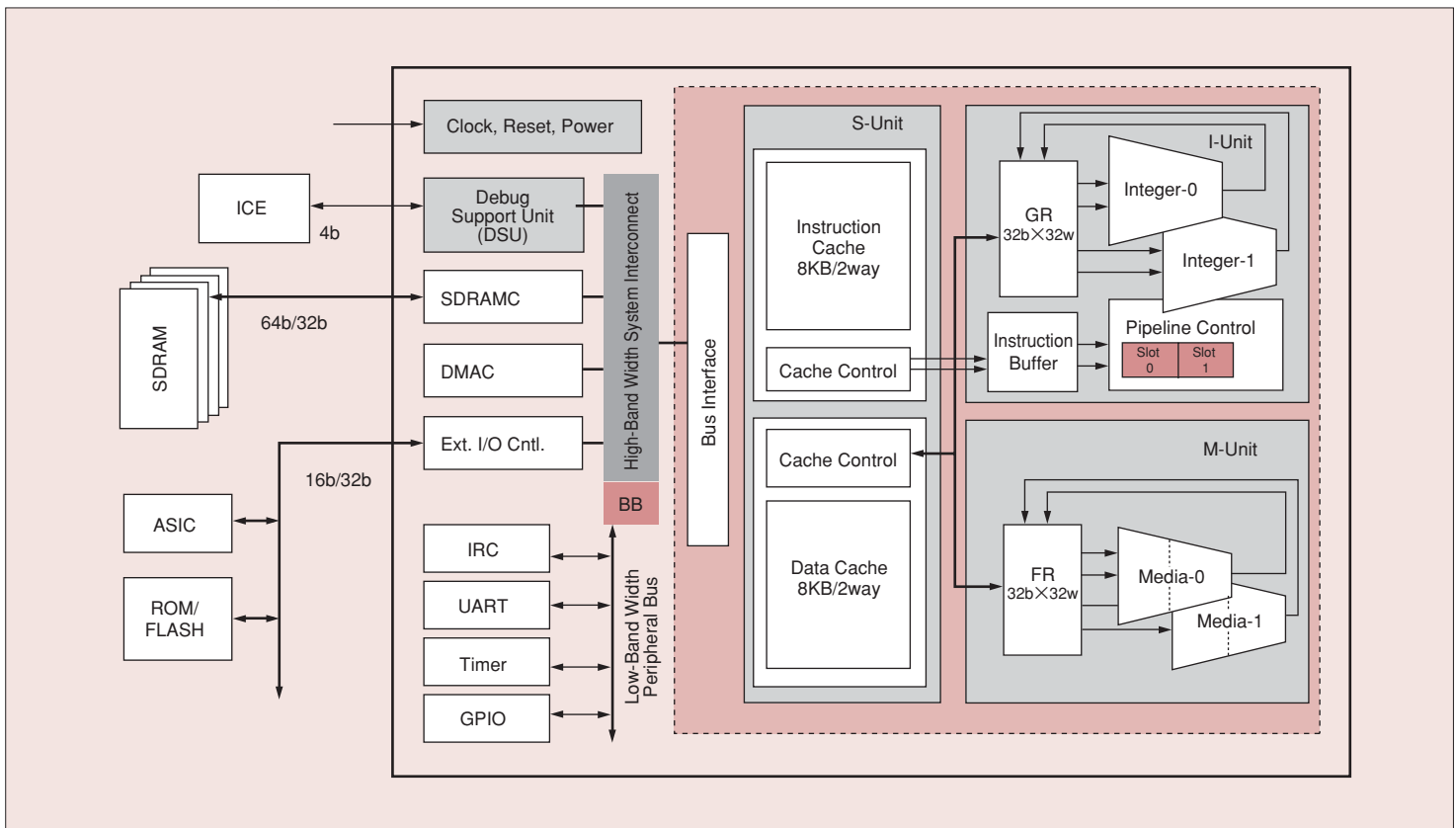
The VDK connects any high-speed bus converted by the FPGA circuit to PCI and other external expansion connectors. It can also convert the high-speed bus to a lower-speed SI (System I ntegration) bus for connection to any lower-speed memory and/or peripheral LSI.

VDK offers the advantages of:

- A complete set of environments for system evaluation and development
- Availability for immediate use via a simple setup procedure
- Support for initial performance and function evaluations through to full-scale application development
- A platform that works with specific ICEs, a wide range of real-time operating systems, and development environments
- Incorporation of a main board compatible with FR500 CPU board

Fig.4 illustrates FR-V design kit. \*

Figure 3 MB93401A Block Diagram



**NOTES**

- \*1: Composite printers containing the facsimile and copying options integrated with conventional printer capability
- \*2: Printers for print images transmitted from a PC or other application-running host machine. As these printers are not required to support PDL analysis or image creation, they are available at lower prices. Practically speaking, they are the opposite of "command base" printers.
- \*3: Units to decode, manipulate, and/or additionally process data input for delivery (such as units to decode and manipulate JPEG

- data captured in a memory card and then deliver it as video).
- \*4: axLinux is a Linux-based operating system developed and offered by AXE, Inc., Linux vender in Japan, for embedded and mobile applications.
- \*5: The VDK for the FR400 is available as a CPU board (MB93091-CB10) and general-purpose main board (MB93090-MB00) configured together in a set.

\* SOFTUNE and REALOS are trademarks of FUJITSU LIMITED.

**Figure 4** FR-V Design Kit (VDK)

